MF794-03

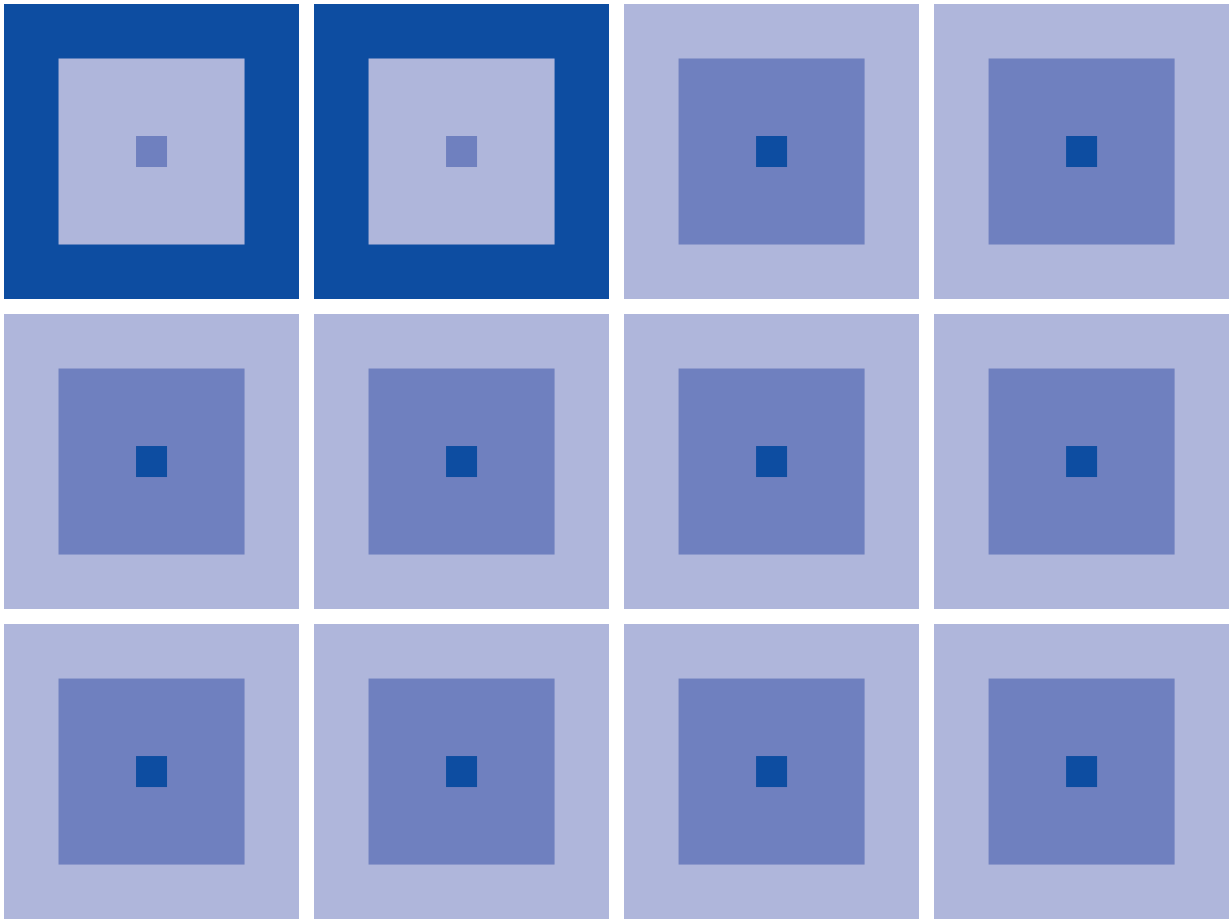
EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

S1C62920

Technical Manual

S1C62920 Technical Hardware



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The information of the product number change

Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

Devices

S1 C 60N01 F 0A01 00

- 00 — Packing specification
- 0A01 — Specification
- F — Package (D: die form; F: QFP)
- 60N01 — Model number
- C — Model name (C: microcomputer, digital products)
- S1 — Product classification (S1: semiconductor)

Development tools

S5U1 C 60R08 D1 1 00

- 00 — Packing specification
- 1 — Version (1: Version 1 *2)
- D1 — Tool type (D1: Development Tool *1)
- 60R08 — Corresponding model number (60R08: for S1C60R08)
- C — Tool classification (C: microcomputer use)
- S5U1 — Product classification (S5U1: development tool for semiconductor products)

*1: For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)
*2: Actual versions are not written in the manuals.

Comparison table between new and previous number

S1C60 Family processors

Previous No.	New No.
E0C6001	S1C60N01
E0C6002	S1C60N02
E0C6003	S1C60N03
E0C6004	S1C60N04
E0C6005	S1C60N05
E0C6006	S1C60N06
E0C6007	S1C60N07
E0C6008	S1C60N08
E0C6009	S1C60N09
E0C6011	S1C60N11
E0C6013	S1C60N13
E0C6014	S1C60140
E0C60R08	S1C60R08

S1C62 Family processors

Previous No.	New No.
E0C621A	S1C621A0
E0C6215	S1C62150
E0C621C	S1C621C0
E0C6S27	S1C6S2N7
E0C6S37	S1C6S3N7
E0C623A	S1C6N3A0
E0C623E	S1C6N3E0
E0C6S32	S1C6S3N2
E0C6233	S1C62N33
E0C6235	S1C62N35
E0C623B	S1C6N3B0
E0C6244	S1C62440
E0C624A	S1C624A0
E0C6S46	S1C6S460

Previous No.	New No.
E0C6247	S1C62470
E0C6248	S1C62480
E0C6S48	S1C6S480
E0C624C	S1C624C0
E0C6251	S1C62N51
E0C6256	S1C62560
E0C6292	S1C62920
E0C6262	S1C62N62
E0C6266	S1C62660
E0C6274	S1C62740
E0C6281	S1C62N81
E0C6282	S1C62N82
E0C62M2	S1C62M20
E0C62T3	S1C62T30

Comparison table between new and previous number of development tools

Development tools for the S1C60/62 Family

Previous No.	New No.
ASM62	S5U1C62000A
DEV6001	S5U1C60N01D
DEV6002	S5U1C60N02D
DEV6003	S5U1C60N03D
DEV6004	S5U1C60N04D
DEV6005	S5U1C60N05D
DEV6006	S5U1C60N06D
DEV6007	S5U1C60N07D
DEV6008	S5U1C60N08D
DEV6009	S5U1C60N09D
DEV6011	S5U1C60N11D
DEV60R08	S5U1C60R08D
DEV621A	S5U1C621A0D
DEV621C	S5U1C621C0D
DEV623B	S5U1C623B0D
DEV6244	S5U1C62440D
DEV624A	S5U1C624A0D
DEV624C	S5U1C624C0D
DEV6248	S5U1C62480D
DEV6247	S5U1C62470D

Previous No.	New No.
DEV6262	S5U1C62620D
DEV6266	S5U1C62660D
DEV6274	S5U1C62740D
DEV6292	S5U1C62920D
DEV62M2	S5U1C62M20D
DEV6233	S5U1C62N33D
DEV6235	S5U1C62N35D
DEV6251	S5U1C62N51D
DEV6256	S5U1C62560D
DEV6281	S5U1C62N81D
DEV6282	S5U1C62N82D
DEV6S27	S5U1C6S2N7D
DEV6S32	S5U1C6S3N2D
DEV6S37	S5U1C6S3N7D
EVA6008	S5U1C60N08E
EVA6011	S5U1C60N11E
EVA621AR	S5U1C621A0E2
EVA621C	S5U1C621C0E
EVA6237	S5U1C62N37E
EVA623A	S5U1C623A0E

Previous No.	New No.
EVA623B	S5U1C623B0E
EVA623E	S5U1C623E0E
EVA6247	S5U1C62470E
EVA6248	S5U1C62480E
EVA6251R	S5U1C62N51E1
EVA6256	S5U1C62N56E
EVA6262	S5U1C62620E
EVA6266	S5U1C62660E
EVA6274	S5U1C62740E
EVA6281	S5U1C62N81E
EVA6282	S5U1C62N82E
EVA62M1	S5U1C62M10E
EVA62T3	S5U1C62T30E
EVA6S27	S5U1C6S2N7E
EVA6S32R	S5U1C6S3N2E2
ICE62R	S5U1C62000H
KIT6003	S5U1C60N03K
KIT6004	S5U1C60N04K
KIT6007	S5U1C60N07K

S1C62920 Technical Manual

PREFACE

This manual explains the function of the S1C62920, the circuit configurations, and details the controlling method.

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CHAPTER 1 OVERVIEW

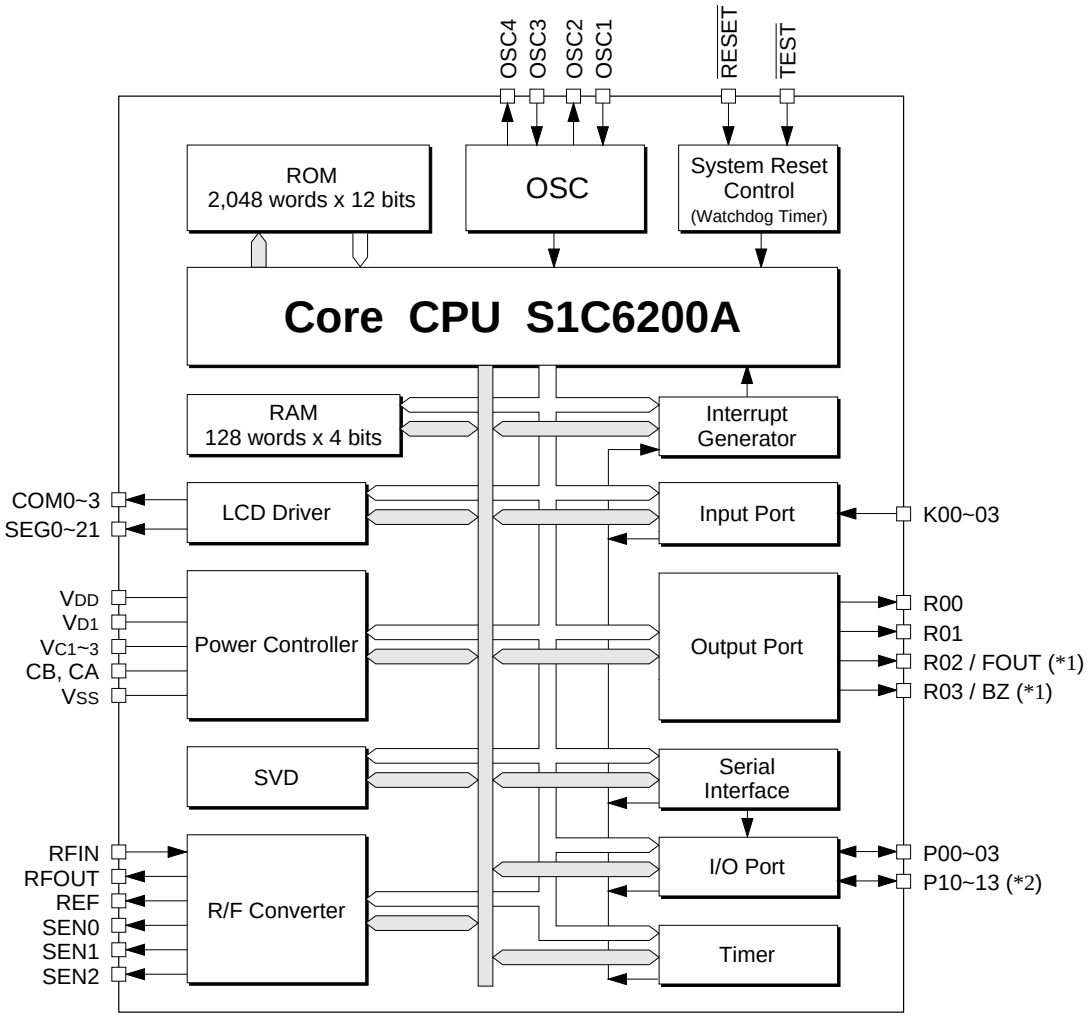
The S1C62920 is a single-chip microcomputer made up of the 4-bit core CPU S1C6200A, ROM (2,048 words, 12 bits to a word), RAM (128 words, 4 bits to a word), R/F converter, SVD circuit, watchdog timer and time base counter.
The S1C62920 is most suitable for controllers with temperature measurement functions, such as a heat control unit.

1.1 Features

OSC1 oscillation circuit	Crystal oscillation circuit: 32.768 kHz (Typ.)		
OSC3 oscillation circuit	Ceramic or CR oscillation circuit (*1): 1 MHz (Typ.)		
Instruction set	108 types		
Instruction execution time .. (differ depending on instruction)	During operation at 32 kHz:	153 µsec, 214 µsec, 366 µsec	
	During operation at 1 MHz:	5 µsec, 7 µsec, 12 µsec	
ROM capacity	2,048 words × 12 bits		
RAM capacity	128 words × 4 bits		
Input port	4 bits (Pull up resistors may be supplemented *1)		
Output port	4 bits (Complementary output or Nch open drain output may be selected *1) May be set to buzzer, clock outputs (*1)		
I/O port	8 bits (Pull up resistors that function during input mode may be supplemented *1) May be switched to serial I/O port (*2)		
LCD driver	22 segments × 2 to 4 commons 1/2–1/4 duty dynamic drive may be selected (*1)		
Serial interface	1 port (Clock synchronous type)		
R/F converter	1 reference resistance × 3 sensors, 16-bit counter DC bias sensor may be connected		
Time base counter	Clock timer: 1 system		
Watchdog timer	Built-in		
SVD circuit ..... (supply voltage detection)	One of thefollowing may be set: 2.4 V, 2.5 V, 2.6 V, 2.7 V (*1)		
External interrupt	Input port interrupt:	1 system	
Internal interrupt	Clock timer interrupt:	1 system	
	R/F converter interrupt:	1 system	
	Serial interface interrupt:	1 system	
Supply voltage	2.2–5.5 V		
Current consumption	During HALT:	2.0 µA	(3 V, Typ.)
	During operation:	5.0 µA	(3 V, 32 kHz, Typ.)
		270 µA	(3 V, 1 MHz, Typ.)
Package	QFP6-64pin, QFP13-64pin (plastic) or chip		

*1 May be selected with mask option.
*2 May be selected with software.

1.2 Block Diagram

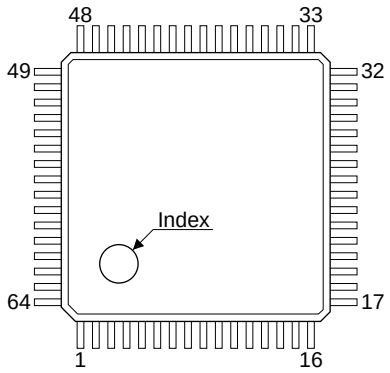


*1 Output is selected by mask option.
*2 P10, P11, P12 and P13 can be set as SIN, SOUT, $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ by software.

Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP6-64pin-S1 (plastic)

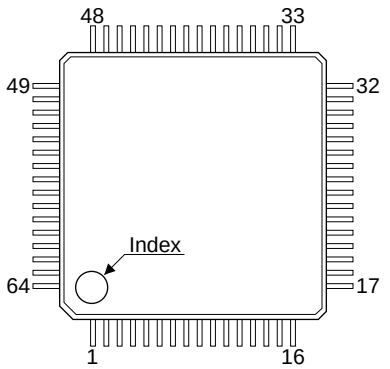


Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	R03	17	P13	33	V_{C2}	49	SEG6
2	R02	18	P12	34	V_{C1}	50	SEG7
3	R01	19	P11	35	V_{C3}	51	SEG8
4	R00	20	P10	36	CA	52	SEG9
5	K03	21	P03	37	CB	53	SEG10
6	K02	22	P02	38	COM3	54	SEG11
7	K01	23	P01	39	COM2	55	SEG12
8	K00	24	P00	40	COM1	56	SEG13
9	N.C.	25	$\overline{RESET}$	41	COM0	57	SEG14
10	REF	26	V_{SS}	42	SEG0	58	SEG15
11	SEN0	27	OSC1	43	SEG1	59	SEG16
12	SEN1	28	OSC2	44	SEG2	60	SEG17
13	SEN2	29	V_{DD}	45	SEG3	61	SEG18
14	RFIN	30	OSC4	46	SEG4	62	SEG19
15	RFOUT	31	OSC3	47	SEG5	63	SEG20
16	N.C.	32	V_{D1}	48	$\overline{TEST}$	64	SEG21

N.C. = No Connection

Fig. 1.3.1 Pin layout diagram (QFP6-64pin-S1)

QFP13-64pin (plastic)



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	R03	17	P13	33	V_{C2}	49	SEG6
2	R02	18	P12	34	V_{C1}	50	SEG7
3	R01	19	P11	35	V_{C3}	51	SEG8
4	R00	20	P10	36	CA	52	SEG9
5	K03	21	P03	37	CB	53	SEG10
6	K02	22	P02	38	COM3	54	SEG11
7	K01	23	P01	39	COM2	55	SEG12
8	K00	24	P00	40	COM1	56	SEG13
9	N.C.	25	$\overline{RESET}$	41	COM0	57	SEG14
10	REF	26	V_{SS}	42	SEG0	58	SEG15
11	SEN0	27	OSC1	43	SEG1	59	SEG16
12	SEN1	28	OSC2	44	SEG2	60	SEG17
13	SEN2	29	V_{DD}	45	SEG3	61	SEG18
14	RFIN	30	OSC4	46	SEG4	62	SEG19
15	RFOUT	31	OSC3	47	SEG5	63	SEG20
16	N.C.	32	V_{D1}	48	$\overline{TEST}$	64	SEG21

N.C. = No Connection

Fig. 1.3.2 Pin layout diagram (QFP13-64pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	In/Out	Function
V_{DD}	29	(I)	Power supply pin (+)
V_{SS}	26	(I)	Power supply pin (–)
V_{D1}	32	O	Oscillation and internal logic system regulated voltage output pin
V_{C1}	34	O	LCD system reduced voltage output pin ($V_{C2} \times 1/2$)
V_{C2}	33	I	LCD system supply voltage input pin ($V_{C2} = V_{D1}$ or $V_{C2} = V_{DD}$)
V_{C3}	35	O	LCD system booster voltage output pin ($V_{C2} \times 3/2$)
CA, CB	36, 37	–	Voltage boost/reduction capacitor connecting pin
OSC1	27	I	Crystal oscillation input pin
OSC2	28	O	Crystal oscillation output pin
OSC3	31	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	30	O	Ceramic or CR oscillation output pin (selected by mask option)
COM0~COM3	41~38	O	LCD common output pin (drive duty may be selected from 1/2–1/4 by mask option)
SEG0~SEG21	42~47, 49~64	O	LCD segment output pin (DC output may be selected by mask option)
K00~K03	8~5	I	Input port pin
P00~P03	24~21	I/O	I/O port pin
P10~P13	20~17	I/O	I/O port pin (serial I/O port may be selected by software)
R00, R01	4, 3	O	Output port pin
R02	2	O	Output port pin (DC or FOUT output may be selected by mask option)
R03	1	O	Output port pin (DC or BZ output may be selected by mask option)
REF	10	O	Reference resistance connecting pin for R/F converter
SEN0, SEN1, SEN2	11, 12, 13	O	Sensor connecting pin for R/F converter
RFIN	14	I	R/F converter CR oscillation input pin
RFOUT	15	O	R/F converter oscillation frequency output pin
$\overline{\text{RESET}}$	25	I	Initial reset input pin
$\overline{\text{TEST}}$	48	I	Testing input pin

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The S1C62920 operating power voltage is as follows:

2.2 V to 5.5 V

The S1C62920 operates when a single power supply within the above range is applied between V_{DD} and V_{SS}. The IC itself can generate the voltage necessary for the internal circuits with the following built-in power supply circuit.

Table 2.1.1 Power supply circuit and output voltage

Circuit	Power supply circuit	Output voltage
Oscillation and internal circuits	Oscillation system regulated voltage circuit	V_{D1}
LCD driver	LCD system voltage boost/reduction circuit	V_{C1}–V_{C3}

Note:
- *External loads cannot be driven by the regulated voltage and voltage boost/reduction circuits' output voltages.*
- *See Chapter 7, "ELECTRICAL CHARACTERISTICS" for voltage values.*

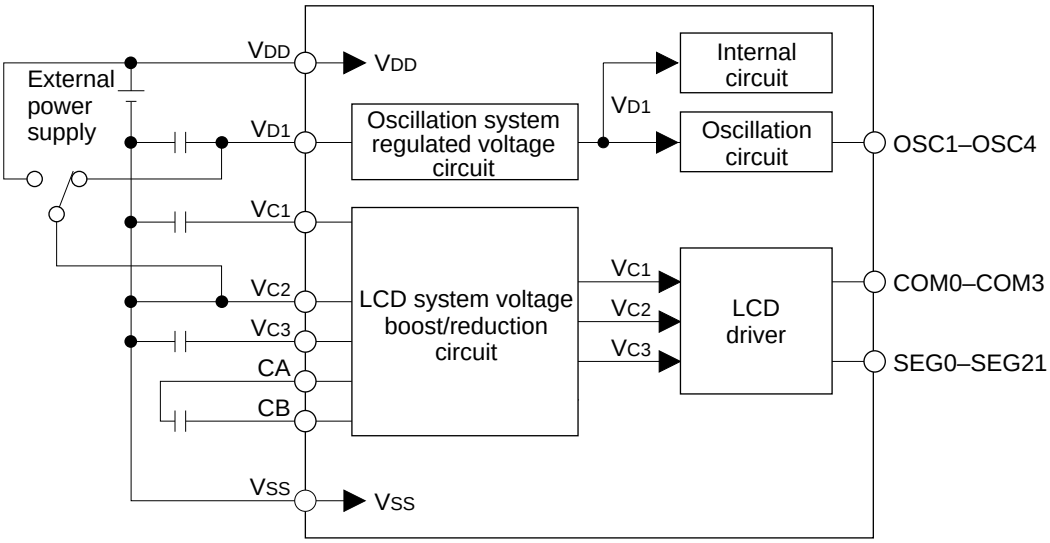


Fig. 2.1.1 Configuration of power supply

2.1.1 Voltage <V_{D1}> for oscillation circuit and internal circuits

V_{D1} is the voltage for the oscillation circuit and the internal logic circuits, and is generated by the oscillation system regulated voltage circuit for stabilizing the oscillation.
Making V_{SS} the standard (GND level), the oscillation system regulated voltage circuit generates V_{D1} from the supply voltage that is input from the V_{DD}–V_{SS} terminals.

2.1.2 Voltage <V_{C1}, V_{C2} and V_{C3}> for LCD driving

V_{C1}, V_{C2} and V_{C3} are the voltages for LCD drive, and are generated by the LCD system voltage boost/reduction circuit to stabilize the display quality.
V_{C2} is generated by connecting the V_{C2} terminal to the V_{DD} or V_{D1} terminal.
The LCD system voltage boost/reduction circuit generates V_{C1} and V_{C3} by transforming V_{C2} into 1/2 and 3/2, respectively.
The following shows V_{C1}–V_{C3} voltages when V_{C2} is connected to the V_{DD} terminal or the V_{D1} terminal :

Terminal connected to V_{C2}	V_{C1}	V_{C2}	V_{C3}	(Recommended operating conditions)
V_{DD} terminal	1/2 V_{DD}	V_{DD}	3/2 V_{DD}	(V_{DD} = 2.2 to 3.6 V)
V_{D1} terminal	approx. 1 V	approx. 2 V	approx. 3 V	(V_{DD} = 2.2 to 5.5 V)

2.2 Initial Reset

To initialize the S1C62920 circuits, initial reset must be executed. There are two ways of doing this.

(1) External initial reset by the $\overline{RESET}$ terminal
(2) Initial reset by the watchdog timer

Be sure to use reset function (1) when turning the power on and be sure to initialize securely. In normal operation, the circuit may be initialized by any of the above two types.

Figure 2.2.1 shows the configuration of the initial reset circuit.

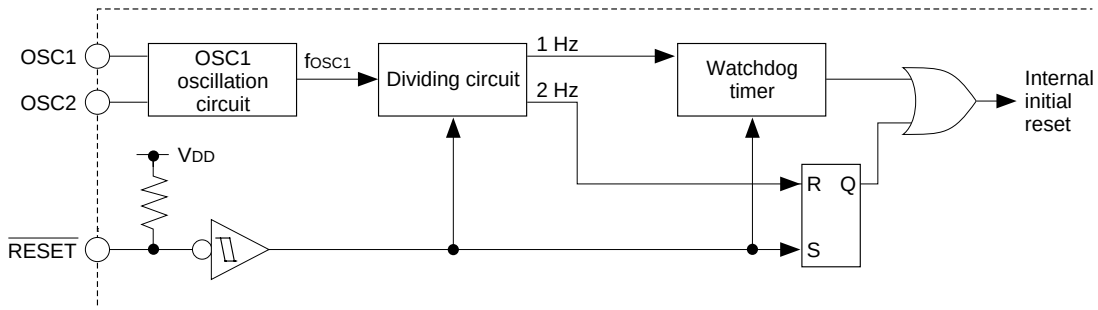


Fig. 2.2.1 Configuration of the initial reset circuit

2.2.1 Reset terminal ($\overline{RESET}$)

Initial reset can be executed externally by setting the reset terminal to a low level (V_{SS}). After that the initial reset is released by setting the reset terminal to a high level (V_{DD}) and the CPU starts operation.
The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 2 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 250 msec (when f_{OSC1} = 32 kHz) is needed until the internal initial reset is released after the reset terminal goes to high level. Be sure to maintain a reset input of 0.1 msec or more.

However, when turning the power on, the reset terminal should be set at a low level as in the timing shown in Figure 2.2.1.1.

The reset terminal should be set to 0.1·V_{DD} or less (low level) until the supply voltage becomes 2.2 V or more.
After that, a level of 0.4·V_{DD} or less should be maintained more than 2.0 msec.

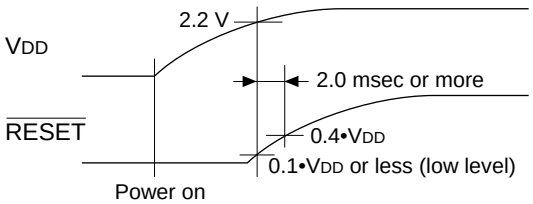


Fig. 2.2.1.1 Initial reset at power on

2.2.2 Watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See Section 4.2, "Resetting Watchdog Timer", for details.
As with the oscillation detection circuit, you should not do an initial reset at power-on using this function.

2.2.3 Internal register at initial resetting

Initial reset initializes the CPU as shown in the table below.

Table 2.2.3.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register IX	IX	9	Undefined
Index register IY	IY	9	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	—	*

* See Section 4.1, "Memory Map".

2.3 Test Terminal ($\overline{TEST}$)

This terminal is used at the time of the factory inspection of the IC. During normal operation, connect the $\overline{TEST}$ to V_{DD}.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C62920 employs the 4-bit core CPU S1C6200A for the CPU, so that register configuration, instructions and so forth are virtually identical to those in other family processors using the S1C6200A.
Refer to "S1C6200/6200A Core CPU Manual" for details about the S1C6200A.
Note the following points with regard to the S1C62920:

(1) The SLEEP operation is not assumed, so the SLP instruction cannot be used.

(2) RAM is set up to one page, so only the one low-order bit is valid for the page portion (XP, YP) of the index register that specifies addresses. (The three high-order bits are ignored.)

3.2 ROM

The built-in ROM, a mask ROM for loading the program, has a capacity of 2,048 steps, 12 bits each. The program area is configured of 8 pages (0–7) with 256 steps each (00H–FFH). After initial reset, the program beginning address is page 1, step 00H. The interrupt vector is allocated to each page 1, steps 02H–0BH.

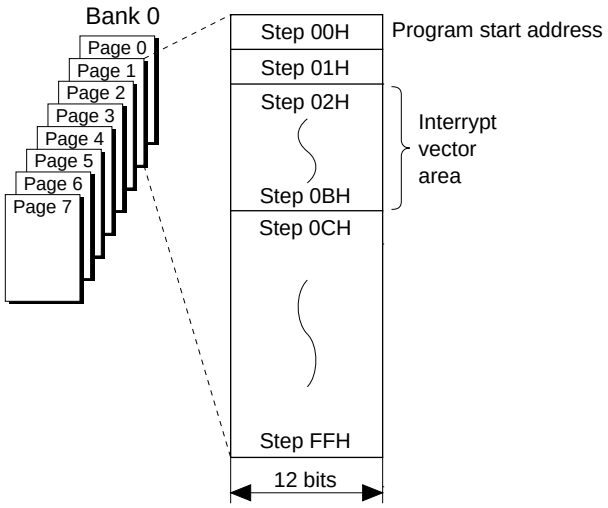


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory storing a variety of data, has a capacity of 128 words, each of four bits. When programming, keep the following points in mind.

(1) Part of the data memory can be used as stack area when subroutine calls and saving registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words of the stack area.

(3) The data memory 000H–00FH is for the register pointers (RP), and is the addressable memory register area.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the S1C62920 are memory mapped, and interfaced with the CPU. Thus, all the peripheral circuits can be controlled by using the memory operation command to access the I/O memory in the memory map.
The following sections describe how the peripheral circuits operation.

4.1 Memory Map

Data memory of the S1C62920 has an address space of 192 words, of which 32 words are allocated to display memory and 32 words to I/O memory.
Figure 4.1.1 presents the overall memory maps of the S1C62920, and Tables 4.1.1(a)–(c) the peripheral circuits' (I/O space) memory maps.
In the S1C62920 the same I/O memory has been laid out for each page 80H–FCH. As a result, the I/O memory can be accessed without changing over the data memory page. The same result is obtained for I/O memory changes and for readable/writable address references, no matter on what page it is done.

Note: Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

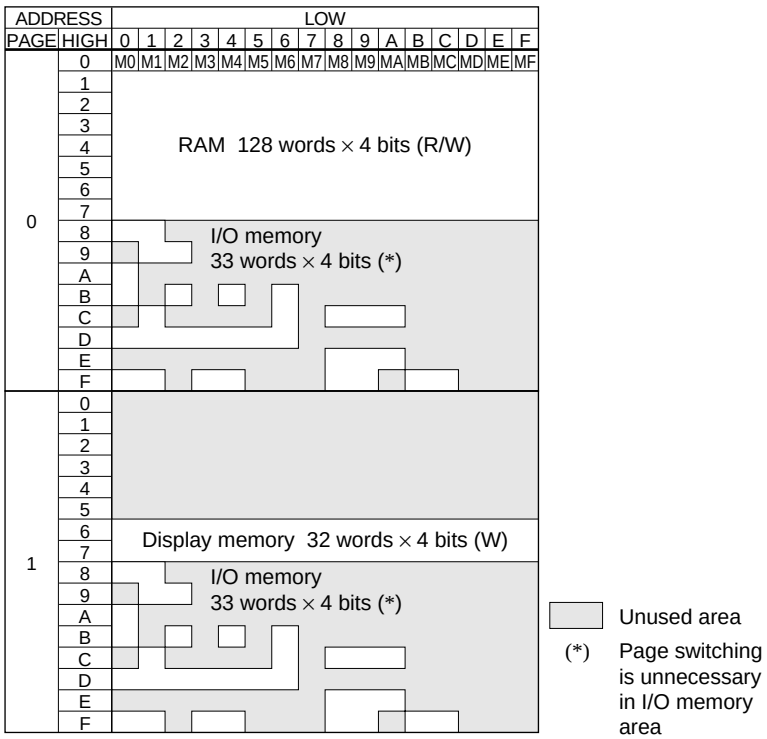


Fig. 4.1.1 Memory map

Table 4.1.1(a) I/O memory map (80H–B6H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
80H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	Supply voltage detaction data
					SVDON	0	On	Off	SVD circuit On/Off
81H	0	0	CLKCHG	OSCC	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 scillation On/Off
91H	K03	K02	K01	K00	K03	– *2	High	Low	Input port K00–K03
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	Input comparison register (K00–K03)
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
A0H	R03 (BZ)	R02 (FOUT)	R01	R00	R03	0	High	Low	Output port R03
					(BZ)	0	On	Off	BZ On/Off (selected by mask option)
					R02	0	High	Low	Output port R02
	R/W				(FOUT)	0	On	Off	FOUT On/Off (selected by mask option)
					R01	0	High	Low	Output port R01
					R00	0	High	Low	Output port R00
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	I/O control register (P00–P03)
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
B2H	P03	P02	P01	P00	P03	1	High	Low	I/O port P00–P03
					P02	1	High	Low	
	R/W				P01	1	High	Low	
					P00	1	High	Low	
B4H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	I/O control register (P10–P13)
					IOC12	0	Output	Input	
	R/W				IOC11	0	Output	Input	
					IOC10	0	Output	Input	
B6H	P13	P12	P11	P10	P13	1	High	Low	I/O port P10–P13
					P12	1	High	Low	
	R/W				P11	1	High	Low	
					P10	1	High	Low	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.1.1(b) I/O memory map (C1H–D6H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C1H	0	0	LOFF	LPWR	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		LOFF	0	All off	Normal	LCD display control
					LPWR	0	On	Off	LCD power supply On/Off
C6H	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST*5	Reset	Reset	–	Watchdog timer reset
C8H	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST*5	Reset	Reset	–	Clock timer reset
C9H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
CAH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
D0H	DBGOS	RFDBG	RFCLK	0	DBGOS	0	Sensor	Ref.-R	R/F converter debugging element selection
					RFDBG	0	Debug	Normal	R/F converter debug mode selection
	R/W			R	RFCLK	0	OSC3	OSC1	R/F converter clock source selection
					0 *5	– *2			Unused
D1H	0	0	SENS1	SENS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		SENS1	0			R/F converter sensor selection
					SENS0	0			0=SEN0, 1=SEN1, 2&3=SEN2
D2H	OVTBC	OVMC	RFRUN	0	OVTBC	0	Overflow	Non-over	Time base counter overflow flag
					OVMC	0	Overflow	Non-over	Measurement counter overflow flag
	R/W			R	RFRUN	0	Run	Stop	R/F converter Run/Stop
					0 *5	– *2			Unused
D3H	MC03	MC02	MC01	MC00	MC03	– *3			Measurement counter MC00–MC03
					MC02	– *3			
	R/W				MC01	– *3			
					MC00	– *3			
D4H	MC07	MC06	MC05	MC04	MC07	– *3			Measurement counter MC04–MC07
					MC06	– *3			
	R/W				MC05	– *3			
					MC04	– *3			
D5H	MC11	MC10	MC09	MC08	MC11	– *3			Measurement counter MC08–MC11
					MC10	– *3			
	R/W				MC09	– *3			
					MC08	– *3			
D6H	MC15	MC14	MC13	MC12	MC15	– *3			Measurement counter MC12–MC15
					MC14	– *3			
	R/W				MC13	– *3			
					MC12	– *3			

Table 4.1.1(c) I/O memory map (E8H–FCH)

address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E8H	SCS0	0	SCTRG	ESIF	SCS0	0	FOUT	Slave	Serial I/F clock mode selection
					0 *5	– *2			Unused
					SCTRG(W)	– *2	Trigger	–	Serial I/F clock trigger (writing)
	R/W	R	R/W		SCTRG(R)	0	Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF port	I/O port	P1 port function selection
E9H	SD3	SD2	SD1	SD0	SD3	– *2			MSB
					SD2	– *2			Serial I/F data (low-order 4 bits)
	R/W				SD1	– *2			
					SD0	– *2			LSB
EAH	SD7	SD6	SD5	SD4	SD7	– *2			MSB
					SD6	– *2			Serial I/F data (high-order 4 bits)
	R/W				SD5	– *2			
					SD4	– *2			LSB
F0H	0	0	0	EISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
F1H	0	0	0	EIRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIRF	0	Enable	Mask	Interrupt mask register (R/F converter)
F3H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F4H	0	EIT2	EIT1	EIT0	0 *5	– *2			Unused
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R	R/W			EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
F8H	0	0	0	ISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ISIF *4	0	Yes	No	Interrupt factor flag (Serial I/F)
F9H	0	0	0	IRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IRF *4	0	Yes	No	Interrupt factor flag (R/F converter)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
FCH	0	IT2	IT1	IT0	0 *5	– *2			Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

4.2 Resetting Watchdog Timer

4.2.1 Configuration of watchdog timer

The S1C62920 incorporates a watchdog timer as the source oscillator for OSC1 (dividing clock = 1 Hz). The watchdog timer must be reset cyclically by the software. If reset is not executed in at least 3 or 4 seconds, the initial reset signal is output automatically for the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

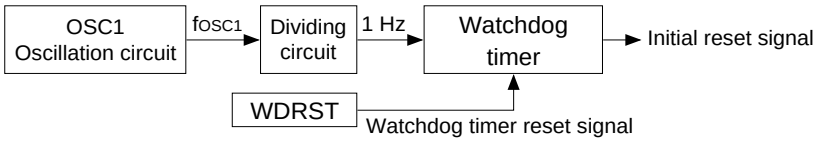


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer, configured of a 2-bit binary counter, generates the initial reset signal internally by overflow of the last stage (1/4 Hz).
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If the HALT status continues for 3 or 4 seconds, the initial reset signal restarts operation.

4.2.2 Control of watchdog timer

Table 4.2.2.1 lists the watchdog timer's control bit and its address.

Table 4.2.2.1 Control bit of watchdog timer

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C6H	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST*5	Reset	Reset	–	Watchdog timer reset

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

WDRST: Watchdog timer reset (C6H•D0)
This is the bit for resetting the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written to WDRST, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.2.3 Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The S1C62920 has two oscillation circuits (OSC1 and OSC3). The OSC1 oscillation circuit generates main clock of 32.768 kHz (Typ.). The OSC3 oscillation circuit generates sub-clock to drive the CPU and some peripheral circuits (serial interface, R/F converter and FOUT output) in high-speed.
Figure 4.3.1.1 is the block diagram of this oscillation system.

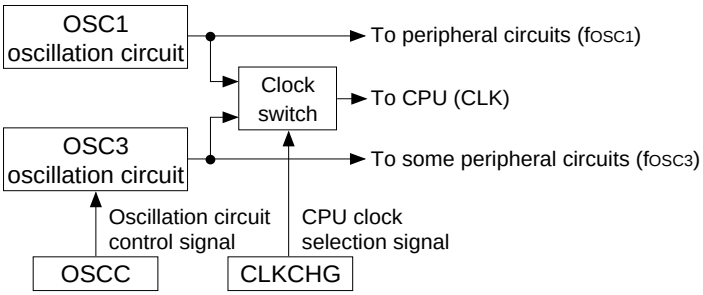


Fig. 4.3.1.1 Oscillation system

At initial reset, the OSC1 oscillation circuit is selected for the CPU operating clock and the OSC3 oscillation circuit is in stop status.
Turning the OSC3 oscillation circuit on and off and switching the system clock (OSC1↔OSC3) can be controlled by the software. The OSC3 oscillation circuit should be used when the CPU and some peripheral circuits need high-speed operation. If it is not necessary, stop the OSC3 oscillation and use OSC1 as the operating clock to reduce current consumption.

4.3.2 OSC1 oscillation circuit

The OSC1 oscillation circuit generates 32.768 kHz (Typ.) system clock.
The OSC1 oscillation clock is used as the system clock when the CPU and the peripheral circuits operate in low-speed (low current consumption). Furthermore, even when OSC3 is used as the system clock, it is still used as the clock source for the clock timer and the watchdog timer.
Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

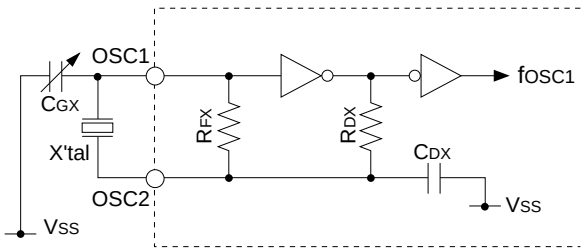
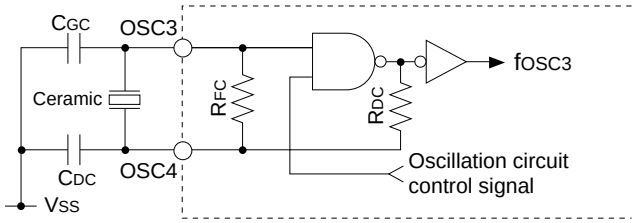


Fig. 4.3.2.1 OSC1 oscillation circuit

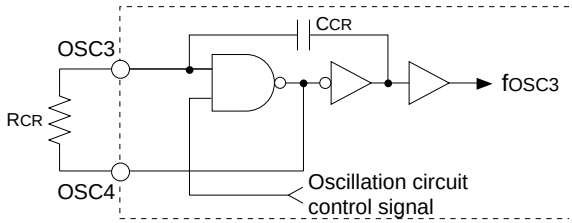
As Figure 4.3.2.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator X'tal (Typ. 32.768 kHz) between terminals OSC1 and OSC2 to the trimmer capacitor CGX (5–25 pF) between terminals OSC1 and VSS.

4.3.3 OSC3 oscillation circuit

The OSC3 oscillation circuit generates the system clock to drive the CPU and some peripheral circuits (serial interface, R/F converter and FOUT output) in high-speed.
Either ceramic oscillation or CR oscillation can be selected by the mask option for the oscillation circuit type.
Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.



(a) Ceramic oscillation circuit



(b) CR oscillation circuit

Fig. 4.3.3.1 OSC3 oscillation circuit

When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Max. 1 MHz) between terminals OSC3 and OSC4 to the two capacitors (C_{GC} and C_{DC}) located between terminals OSC3 and OSC4 and V_{SS}.
When CR oscillation is selected, the CR oscillation circuit can be configured simply by connecting the resistor (R_{CR}) between terminals OSC3 and OSC4.

4.3.4 CPU clock switching

The CPU system clock can be switched between OSC1 and OSC3 by the software.
When the CPU operates by OSC1, turning the OSC3 oscillation circuit off can save power.
If high-speed operation is required, turn the OSC3 oscillation circuit on and switch the system clock to OSC3. In this case, switch the clock to OSC3 after 5 msec or more time has elapsed since this time is necessary for stabilizing the oscillation after turning the OSC3 oscillation circuit on. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
When switching from OSC3 to OSC1, turn the OSC3 oscillation circuit off immediately after the clock is switched to OSC1.

4.3.5 Clock frequency and instruction execution time

Table 4.3.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.3.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (µsec)		
	5-clock instruction	7-clock instruction	12-clock instruction
OSC1: 32.768 kHz	152.6	213.6	366.2
OSC3: 1 MHz	5.0	7.0	12.0

4.3.6 Control of oscillation circuit

Table 4.3.6.1 lists the control bits and their addresses for the oscillation circuit.

Table 4.3.6.1 Control bits of oscillation circuit

Address *7	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
81H	0	0	CLKCHG	OSCC	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

OSCC: OSC3 oscillation ON/OFF (81H•D0)

Controls oscillation ON / OFF for the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When it is necessary to operate the CPU and some peripheral circuits (serial interface, R / F converter, FOUT output) at high speed, set OSCC to "1". At other times, set it to "0" to resume current consumption.
At initial reset, this register is set to "0".

CLKCHG: CPU clock switch (81H•D1)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
When switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON (OSCC = "1"). This time is necessary to stabilize the OSC3 oscillation.
At initial reset, this register is set to "0".

4.3.7 Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

OSC1 → OSC3
1. Set OSCC to "1" (OSC3 oscillation ON)
2. Maintain 5 msec or more
3. Set CLKCHG to "1" (OSC1 → OSC3)

OSC3 → OSC1
1. Set CLKCHG to "0" (OSC3 → OSC1)
2. Set OSCC to "0" (OSC3 oscillation OFF)

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for turning the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) If it is not necessary to operate the CPU in high-speed and the OSC3 clock is not needed for some peripheral circuits, turn the OSC3 oscillation circuit off (CLKCHG = "0", OSCC = "0") to reduce current consumption.

4.4 Input Ports (K00–K03)

4.4.1 Configuration of input ports

The S1C62920 has 4 bits input ports that include Schmitt trigger functions. Each of the input port terminals (K00–K03) provides internal pull up resistor. Pull up resistor can be selected for each bit with the mask option.
Figure 4.4.1.1 shows the configuration of input port.

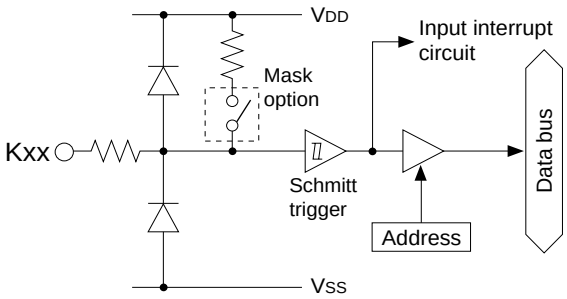


Fig. 4.4.1.1 Configuration of input port

Each of the input port terminals is directly connected to the data bus via a 3-state buffer, and the status of the input signal at the time of the input port reading is loaded as an input data.

4.4.2 Mask option

Internal pull up resistor can be selected for each of the 4 bits of the input ports (K00–K03) with the input port mask option.
Selection of "With pull up resistor" with the mask option suits input from the push switch, key matrix, and so forth.
When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times$ 1.6 [sec]
R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs. In this case, take care that the floating status does not occur for the input.

Select "With pull up resistor" for input ports that are not being used.

All 4 bits of the input ports (K00–K03) provide the interrupt function. It is possible to set whether or not the interrupt will be used by the mask option.

4.4.3 Interrupt function

All 4 bits of the input ports (K00–K03) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, It is possible to set whether or not the interrupt will be used by the mask option.
Figure 4.4.3.1 shows the configuration of K00–K03 interrupt circuit.

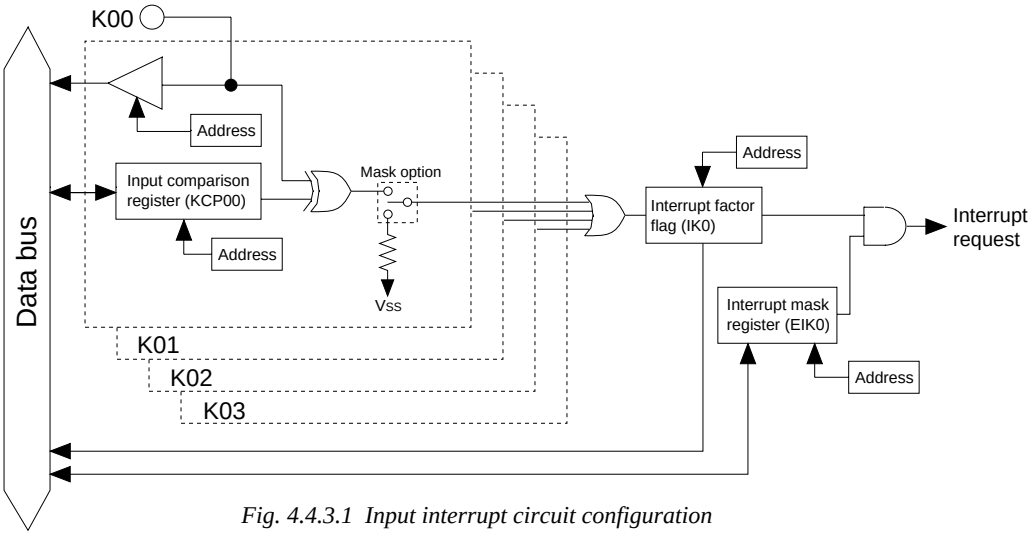


Fig. 4.4.3.1 Input interrupt circuit configuration

The input comparison register (KCP) are individually set for the input ports K00–K03, and can specify the interrupt timing.
The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison register (KCP00–KCP03).
By setting the condition, the interrupt for K00–K03 (4 bits unit) are generated when an input port in which an interrupt has been enabled by the mask option and the content of the input comparison register have been changed from matching to no matching.
The interrupt mask register EIK0 enables the interrupt mask to be selected for K00–K03.
When the interrupt is generated, the interrupt factor flag (IK0) is set to "1".
Figure 4.4.3.2 shows an example of an interrupt for K00–K03.

Input interrupt mask option settings

K03	K02	K01	K00
Use	Use	Use	Not use

Input comparison register

KCP03	KCP02	KCP01	KCP00
1	0	1	0

With the above setting, the interrupt of K00–K03 is generated under the following condition:

Input port

(1)

K03	K02	K01	K00
1	0	1	0

(Initial value)

↓

(2)

K03	K02	K01	K00
1	0	1	1

↓

(3)

K03	K02	K01	K00
0	0	1	1

→ Interrupt generation
Because K00 interrupt is not used, an interrupt will be generated when matching does not occur between the contents of the 3 bits K01–K03 and the 3 bits input comparison register KCP01–KCP03.

↓

(4)

K03	K02	K01	K00
0	1	1	1

Fig. 4.4.3.2 Example of interrupt of K00–K03

K00 interrupt is not used by the mask option setting, so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminal the interrupt used no longer matches the data of the input comparison register, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison register from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals which interrupt is not used do not affect the conditions for interrupt generation.

4.4.4 Control of input ports

Table 4.4.4.1 lists the input ports control bits and their addresses.

Table 4.4.4.1 Input port control bits

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
91H	K03	K02	K01	K00	K03	– *2	High	Low	Input port K00–K03
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	Input comparison register (K00–K03)
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
F3H	0	0	0	EIK0	0 *5	–			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0 *2	Enable	Mask	Interrupt mask register (K00–K03)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

K00–K03: Input port data (91H)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of the 4 bits of the input ports (K00–K03) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for reading, so writing cannot be done.

KCP00–KCP03: Input comparison registers (92H)

Interrupt condition for terminals K00–K03 can be set with this register.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the 4 bits (K00–K03), through the input comparison registers (KCP00–KCP03).
An input comparison is done only with the ports in which the interrupt is used among K00-K03 by the mask option setting.
At initial reset, these registers are set to "1".

EIK0: Interrupt mask register (F3H•D0)

Masking the interrupt of the input port can be selected with this register.

When "1" is written:	Enable
When "0" is written:	Mask
Reading:	Valid

With this registers, masking of the input ports can be selected.
At initial reset, this register is set to "0".

IK0: Interrupt factor flag (FBH•D0)

This flag indicates the occurrence of input interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flag IK0 is associated with K00–K03. From the status of this flag, the software can decide whether an input interrupt has occurred.
This flag is set to "1" by generating the interrupt factor regardless of the interrupt mask register (EIK0) setting.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
This flag is reset when the software reads it.
At initial reset, this flag is set to "0".

4.4.5 Programming notes

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times$ 1.6 [sec]
R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

(2) When the input comparison register (KCP00–KCP03) is set, the interrupt factor flag (IK0) may be set to "1" depending on the status of the input port terminal. Consequently, when setting this register, do it in the DI status (interrupt flag = "0") and then read the interrupt factor flag in order to reset.

(3) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.5 Output Ports (R00–R03)

4.5.1 Configuration of output ports

The S1C62920 has 4 bits general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available; complementary output and Nch open drain output.
Further, the output ports R02 and R03 to be used as special output ports by the software setting.
Figure 4.5.1.1 shows the configuration of the output port.

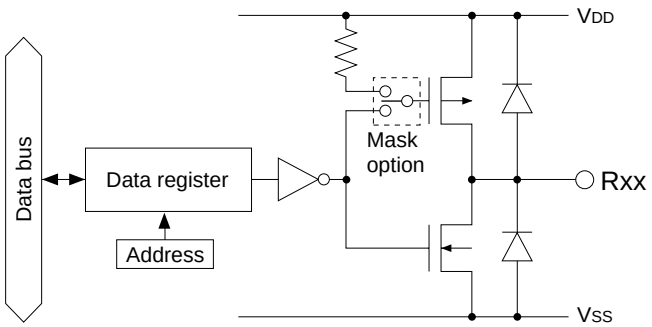


Fig. 4.5.1.1 Configuration of output port

4.5.2 Mask option

(1) Output specification

Output specifications of the output ports can be selected with the mask option.
Output specifications for the output ports (R00–R03) enable selection of either complementary output or Nch open drain output for each of the 4 bits.
The Nch open drain output is suitable for the common output for key matrix and the other outputs.
However, even when Nch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.
Select complementary output set in default for unused output port.

(2) Special output

In addition to the regular DC output, special output can be selected for the output ports R02 and R03 as shown in Table 4.5.2.1 with the mask option. Figure 4.5.2.1 shows the configuration of the special output.

Table 4.5.2.1 Special output

Terminal	Special output
R03	BZ
R02	FOUT

At initial reset, the output terminals are set to low (VSS).
When R02 and R03 are used as the special output ports, turn the signals ON or OFF using the output data register R02 and R03.

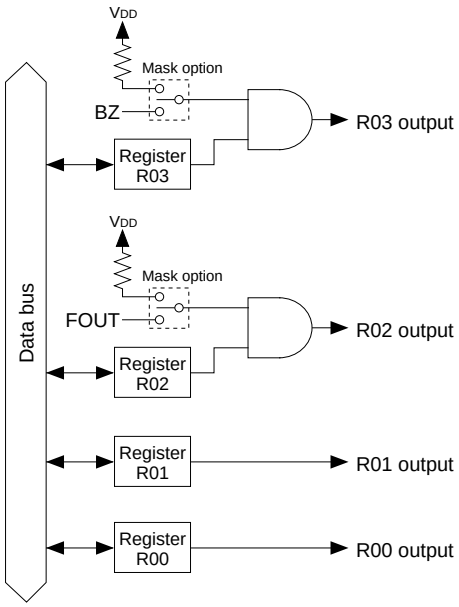


Fig. 4.5.2.1 Configuration of special output

4.5.3 Control of output ports

Table 4.5.3.1 lists the output ports' control bits and their addresses.

Table 4.5.3.1 Control bits of output ports

Address *7	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
A0H	R03 (BZ)	R02 (FOUT)	R01	R00	R03	0	High	Low	Output port R03
					(BZ)	0	On	Off	BZ On/Off (selected by mask option)
					R02	0	High	Low	Output port R02
					(FOUT)	0	On	Off	FOUT On/Off (selected by mask option)
	R/W				R01	0	High	Low	Output port R01
					R00	0	High	Low	Output port R00

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

When not using as special output ports

R00–R03: Output port data (A0H)

Sets the output data for the output ports.

When "1" is written: High output
When "0" is written: Low output
Reading: Valid

The output port terminals output the data written in the corresponding registers (R00–R03) without changing it. When "1" is written in the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
At initial reset, these registers are set to "0".

When using as special output ports

• FOUT (R02)

In order for the S1C62920 to provide a clock signal to an external device, the FOUT signal can be output from the R02 terminal by setting the mask option.
When FOUT output has been set, turning the FOUT signal ON and OFF can be controlled using the R02 register.
When the R02 register is set to "1", the FOUT signal is output from the R02 terminal. When "0" is set, the R02 terminal goes low level (V_{SS}).
FOUT signal frequency can be selected from among 4 types as shown below by setting the mask option.

(1) 512 Hz
(2) 4,096 Hz
(3) f_{OSC1} (OSC1 oscillation frequency)
(4) f_{OSC3} (OSC3 oscillation frequency)

Note: • *FOUT signal frequency that is selected is also used for the clock source in the master mode of the serial interface. Therefore, any one of the 4 types of frequency must be selected for the serial interface even if "FOUT is not used" is selected by the mask option.*
See Section 4.9, "Serial Interface" for details.

• *A hazard may occur when the FOUT signal is turned ON or OFF.*

Figure 4.5.3.1 shows the output waveform of FOUT.

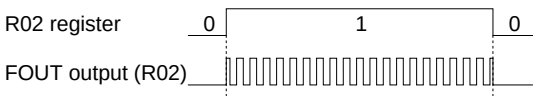


Fig. 4.5.3.1 Output waveform of FOUT

• BZ (R03)

BZ is the buzzer signal output for driving the piezo-electric buzzer, and the BZ output can be selected by the mask option.
When BZ output has been set, turning the BZ signal ON and OFF can be controlled using the R03 register. When the R03 register is set to "1", the BZ signal is output from the R03 terminal. When "0" is set, the R03 terminal goes low level (V_{SS}).
The buzzer frequency can be selected as 2,048 Hz or 4,096 Hz by the mask option.

Note: A hazard may occur when the BZ signal is turned ON or OFF.

Figure 4.5.3.2 shows the output waveform of BZ.

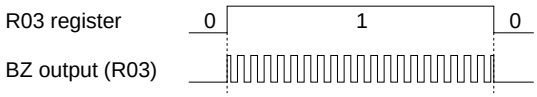


Fig. 4.5.3.2 Output waveform of BZ

4.5.4 Programming notes

(1) When BZ and FOUT are selected, a hazard may be observed in the output waveform when the data of the output register changes.

(2) When selecting f_{OSC3} as the FOUT clock frequency, it is necessary to control the OSC3 oscillation circuit. See Section 4.3, "Oscillation Circuit" for details of the control.

4.6 I/O Ports (P00–P03, P10–P13)

4.6.1 Configuration of I/O ports

The S1C62920 has 8 bits general-purpose I/O ports. Figure 4.6.1.1 shows the configuration of the I/O port. The 8 bits of the I/O ports P00–P03 and P10–P13 can be set to either input mode or output mode (1 bit unit). Modes can be set by writing data to the I/O control register.
Moreover, pull up resistor which is turned ON during input mode can be controlled by the software.
The I/O ports P10–P13 are common used with the input/output ports of the serial interface, and function of these ports can be selected by the software.
See Section 4.9, "Serial Interface", for details of the serial interface.

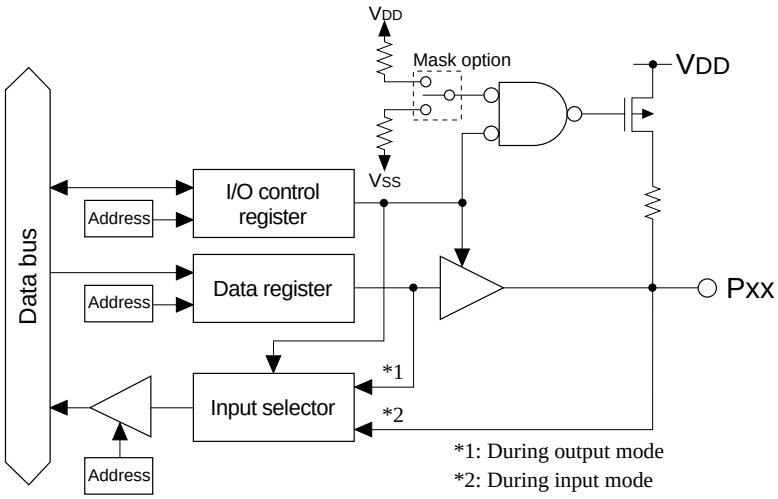


Fig. 4.6.1.1 Configuration of I/O port

4.6.2 Mask option

A pull up resistor that operates during the input mode is built into the I/O ports of the S1C62920. Mask option can set the use or non-use of this pull up. The pull up resistor corresponding to each of P00–P03 and P10–P13 becomes effective by selecting with the mask option.
Even when the serial interface function is selected, mask option (pull up function) of ports that function as input ports (SIN and $\overline{SCLK}$ in the slave mode) is effective.

4.6.3 I/O control registers and input/output mode

Input or output mode can be set for the 8 bits of I/O ports P00–P03 and P10–P13 by writing data into the corresponding I/O control registers IOC00–IOC03 and IOC10–IOC13.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull up has been set by the mask option, the input line is pulled up only during this input mode.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

When the serial interface function is selected, the registers IOC10–IOC12 in the master mode and the registers IOC10–IOC13 in the slave mode can be used as a general register.

At initial reset, the I/O control registers are set to "0", and the I/O port enters the input mode.

4.6.4 Control of I/O ports

Table 4.6.4.1 lists the I/O ports' control bits and their addresses.

Table 4.6.4.1 Control bits of I/O ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	I/O control register (P00–P03)
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
B2H	P03	P02	P01	P00	P03	1	High	Low	I/O port P00–P03
					P02	1	High	Low	
	R/W				P01	1	High	Low	
					P00	1	High	Low	
B4H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	I/O control register (P10–P13)
					IOC12	0	Output	Input	
	R/W				IOC11	0	Output	Input	
					IOC10	0	Output	Input	
B6H	P13	P12	P11	P10	P13	1	High	Low	I/O port P10–P13
					P12	1	High	Low	
	R/W				P11	1	High	Low	
					P10	1	High	Low	
E8H	SCS0	0	SCTRG	ESIF	SCS0	0	FOUT	Slave	Serial I/F clock mode selection
					0 *5	– *2			Unused
					SCTRG(W)	– *2	Trigger	–	Serial I/F clock trigger (writing)
	R/W	R	R/W		SCTRG(R)	0	Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF port	I/O port	P1 port function selection

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

(1) Function selection for ports

ESIF: Serial interface enable (E8H•D0)

Selects function for P10–P13.

When "1" is written: Serial interface input/output port
When "0" is written: I/O port
Reading: Valid

When the serial interface is used, write "1" to this register and when P10–P13 are used as I/O port, write "0". The configuration of the terminals within P10–P13 that are used for the serial interface is decided by the mode selected with the SCS0 register.
At initial reset, this register is set to "0".

(2) I/O port control

P00–P03, P10–P13: I/O port data (B2H, B6H)

I/O port data can be read and output data can be set through these ports.

• ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}).
Port data can be written also in the input mode.

• ***When reading data out***

When "1" is read: High level
When "0" is read: Low level

When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage in the input mode is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When pull up is set by the mask option, the built-in pull up resistor goes ON during input mode, so that the I/O port terminal is pulled up. The gate floating has not occur by the input control signal even if no pull up resistor is set.

When input terminals are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching data during input mode, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times$ 1.6 [sec]
R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

IOC00–IOC03, IOC10–IOC13: I/O control registers (B0H, B4H)

The input and output modes of the I/O ports can be set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in units of one bit. IOC00–IOC03 and IOC10–IOC13 set the mode for P00–P03 and P10–P13, respectively.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are set to "0", so the I/O ports are in the input mode.

4.6.5 Programming note

When input terminals are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching data during input mode, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times$ 1.6 [sec]
R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

4.7 LCD Driver (COM0–COM3, SEG0–SEG21)

4.7.1 Configuration of LCD driver

The S1C62920 has 4 common terminals (COM0–COM3) and 22 segment terminals (SEG0–SEG21), so that it can drive an LCD with a maximum of 88 (22 × 4) segments.
The LCD drive voltage is generated by connecting V_{C2} to supply voltage V_{DD} or V_{D1} generated from the MCU internal circuit.
The driving method is 1/2 duty dynamic drive depending on the four types of potential, V_{SS}, V_{C1}, V_{C2} and V_{C3}. In addition to the 1/2 duty, 1/3 and 1/4 drive duty can be selected by the mask option. The frame frequency is 32 Hz for 1/4 and 1/2 duty, and 42.7 Hz for 1/3 duty (f_{OSC1} = 32.768 kHz).
LCD display ON/OFF may be controlled by the software.

Note: "f_{OSC1}" indicates the oscillation frequency of the OSC1 oscillation circuit.

4.7.2 LCD drive voltage

The LCD drive voltages V_{C1} and V_{C3} are generated internally by transforming V_{C2} into 1/2 and 3/2, respectively. See Section 2.1.2, "Voltage <V_{C1}, V_{C2} and V_{C3}> for LCD driving" for the V_{C1} adjustment method.
The LCD system power circuit that generates V_{C1} and V_{C3} is turned ON and OFF by the LCD power control register LPWR.
By setting LPWR to "1", the LCD system power circuit generates V_{C1} and V_{C3}. When LPWR is set to "0", V_{C1} and V_{C3} become V_{C2} level. In this case, all outputs from the COM terminals and SEG terminals go to V_{C2} level.
To display the LCD, the LCD drive power must be ON by previously setting LPWR to "1".
SEG output ports that are set for DC output by the mask option operate same as the output (R) port regardless of the power ON/OFF control.

4.7.3 LCD display ON/OFF control

In the S1C62920, ON/OFF of the LCD display can be controlled by the LOFF register.
At initial reset, LOFF is set to "0", and the LCD display is set to the ON status.
The LCD power is OFF at initial reset, so the display is actually performed when the LCD power is turned ON (LPWR = "1").
To set all of the LCD display OFF, write "1" to LOFF. With this, the SEG terminals output an OFF waveform.

4.7.4 Display memory area

The display memory is allocated in the data memory area, addresses 60H–7FH in page 1.
Since the display memory is write only, data modification by arithmetic instructions cannot be done.
Correspondence between segment outputs and bits within the display memory can be optionally set by the mask option explained in the next section.

4.7.5 Mask option (drive duty selection and segment allocation)

(1) Drive duty selection

The LCD drive duty can be selected from among 3 types, 1/4, 1/3 and 1/2 duty by the mask option.
Table 4.7.5.1 shows the LCD drive duty setting.

Table 4.7.5.1 LCD drive duty setting

Duty	Terminals used in common	Maximum number of segments	Frame frequency *
1/2	COM0, COM1	44 (22 × 2)	f_{OSC1}/1,024 (32 Hz)
1/3	COM0–COM2	66 (22 × 3)	f_{OSC1}/768 (42.7 Hz)
1/4	COM0–COM3	88 (22 × 4)	f_{OSC1}/1,024 (32 Hz)

* In case of f_{OSC1} = 32.768 kHz

Basically you should select the drive duty with the smallest drive segment number (for example, 1/3 duty for 60 segments and 1/2 duty for 40 segments) from among the drive duties permitting driving of the segment number of the LCD panel.
Figures 4.7.5.1–4.7.5.3 show the dynamic drive waveform for 1/4 duty, 1/3 duty and 1/2 duty.

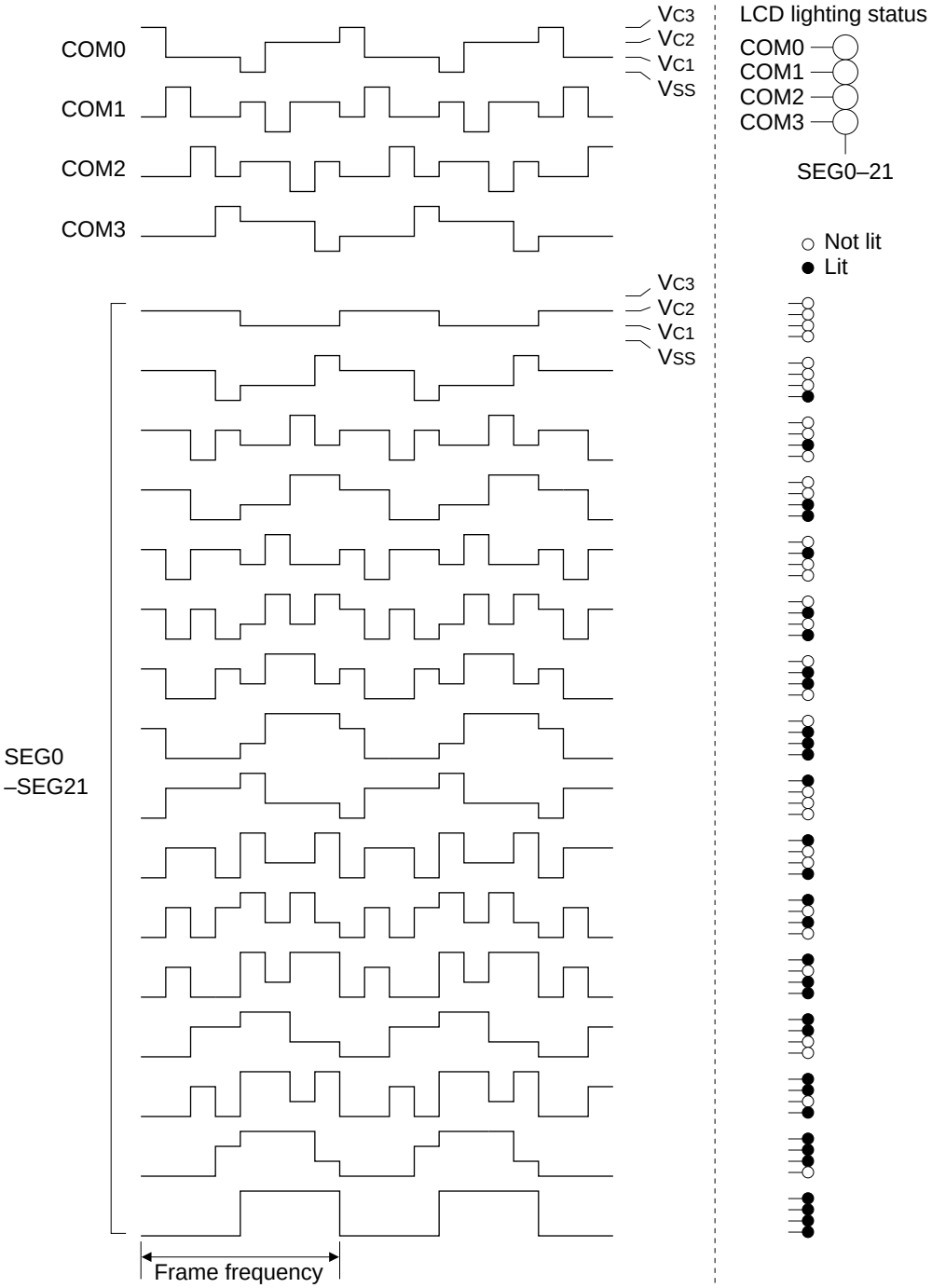


Fig. 4.7.5.1 Drive waveform for 1/4 duty

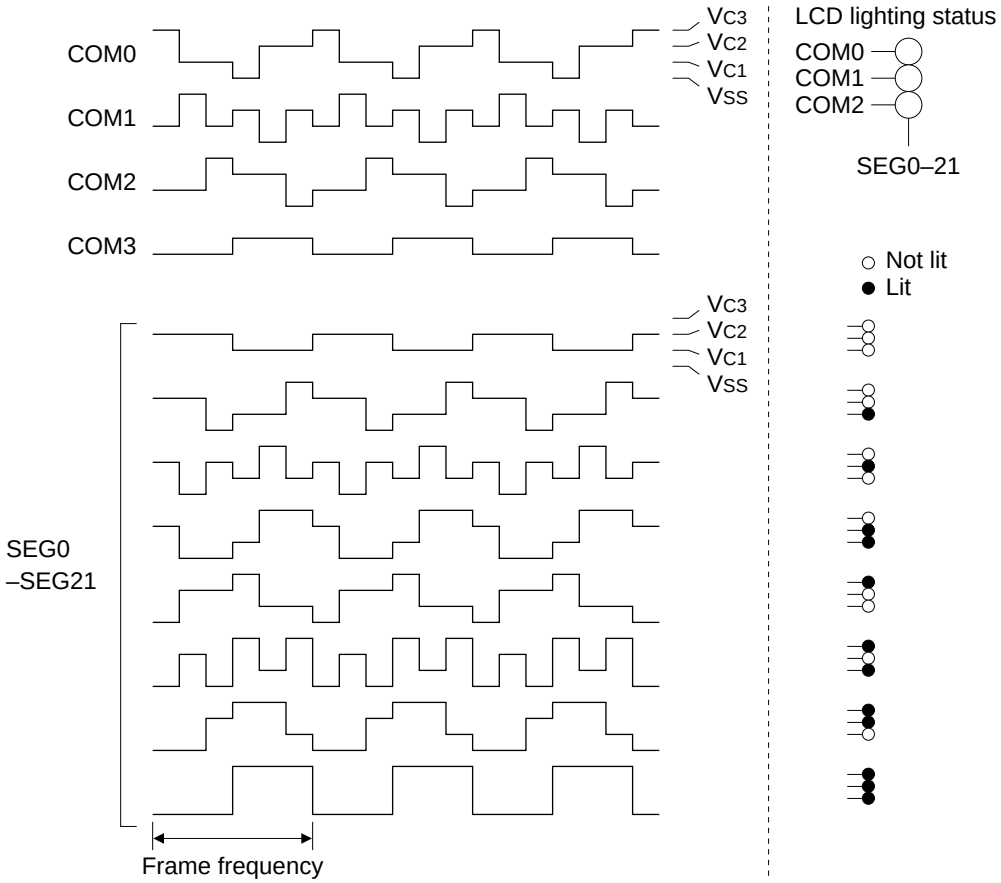


Fig. 4.7.5.2 Drive waveform for 1/3 duty

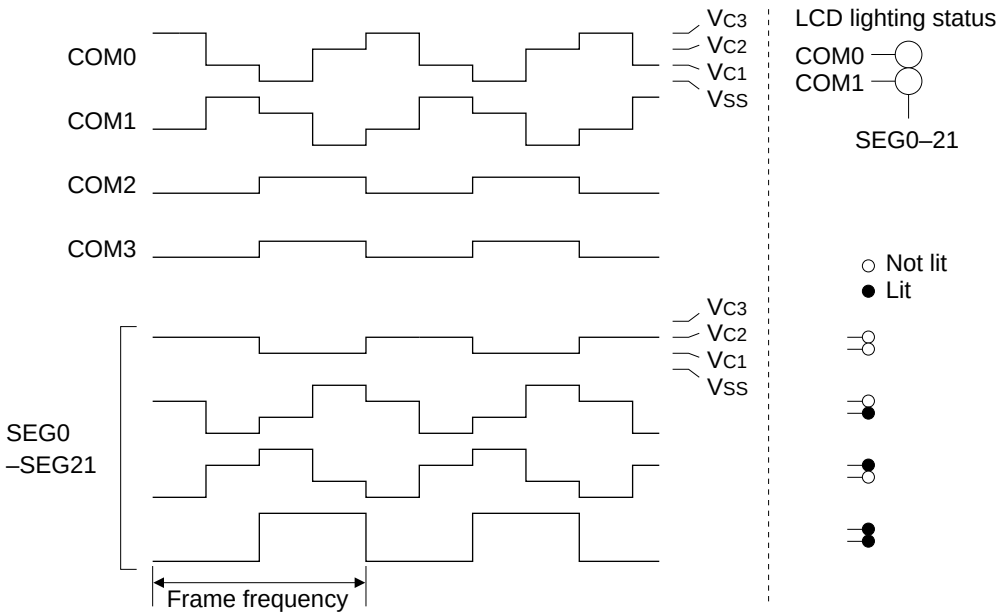


Fig. 4.7.5.3 Drive waveform for 1/2 duty

(2) Segment allocation

The LCD driver has a segment decoder built-in, and the data bit (D0–D3) of the optional address in the display memory area (60H–7FH) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.
The allocated segment displays when the bit for the display memory is set to "1", and goes out when bit is set to "0".

Figure 4.7.5.4 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
7AH	d	c	b	a
7BH	p	g	f	e
7CH	d'	c'	b'	a'
7DH	p'	g'	f'	e'

Display memory allocation

	Common 0	Common 1	Common 2
SEG10	7A, D0 (a)	7B, D1 (f)	7B, D0 (e)
SEG11	7A, D1 (b)	7B, D2 (g)	7A, D3 (d)
SEG12	7D, D1 (f')	7A, D2 (c)	7B, D3 (p)

Pin address allocation

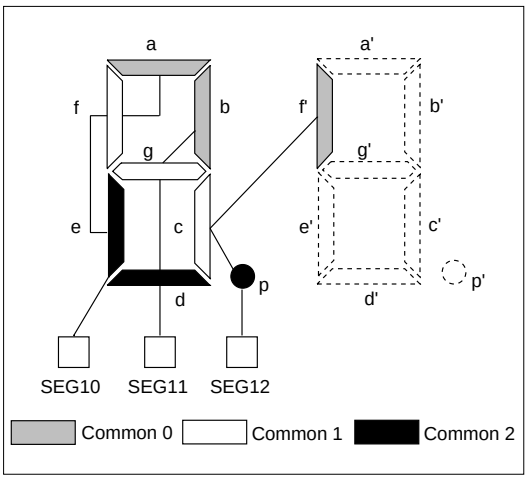


Fig. 4.7.5.4 Segment allocation

(3) Output specification

① The segment terminals (SEG0–SEG21) can be selected with the mask option in each pair for either segment signal output or DC output (V_{DD} and V_{SS} binary output).
When DC output is selected, the data corresponding to COM0 of each segment terminal is output.

② When DC output is selected, either complementary output or Nch open drain output can be selected for each terminal with the mask option.

Note: The terminal pairs are the combination of SEG2 × n and SEG2 × n + 1 (where n is an integer from 0 to 10).

4.7.6 Control of LCD driver

Table 4.7.6.1 shows the LCD driver's control bits and their addresses. Figure 4.7.6.1 shows the display memory map.

Table 4.7.6.1 LCD driver control bits

Address *7	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
C1H	0	0	LOFF	LPWR	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		LOFF	0	All off	Normal	LCD display control
					LPWR	0	On	Off	LCD power supply On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	6	Display memory (32 words x 4 bits) W															
	7																

Fig. 4.7.6.1 Display memory map

LPWR: LCD power supply ON/OFF (C1H•D0)

Controls the LCD power ON and OFF

When "1" is written: Power ON
When "0" is written: Power OFF
Reading: Valid

By writing "1" to LPWR, the LCD power goes ON.
When "0" is written, the LCD power goes OFF and all terminals of the COM output and SEG output become V_{C2} level.
This control does not affect to SEG terminals that have been set for DC output.
At initial reset, this register is set to "0".

LOFF: LCD display control (C1H•D1)

Controls the LCD display

When "1" is written: Display all OFF
When "0" is written: Display ON
Reading: Valid

When "1" is written to LOFF, all LCD dots will fade out; writing "0" will set it back to normal.
All fading out of LCD at LOFF = "1" is due to light out signals and does not affect the content of the segment data memory.
Flashing on the entire LCD panel is performed by this function.
At initial reset, this register is set to "0".

4.7.7 Programming notes

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) Since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

(3) 100 msec or more time is necessary for stabilizing the LCD drive voltages V_{C1} and V_{C3} after setting the LCD power control register LPWR to "1". Be careful of the segment-on right after the power is turned on.

4.8 Clock Timer

4.8.1 Configuration of clock timer

The S1C62920 has a built-in clock timer with OSC1 divided clock (256 Hz) as clock source. The clock timer is configured of a 8-bit binary counter and the timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.8.1.1 is the block diagram for the clock timer.

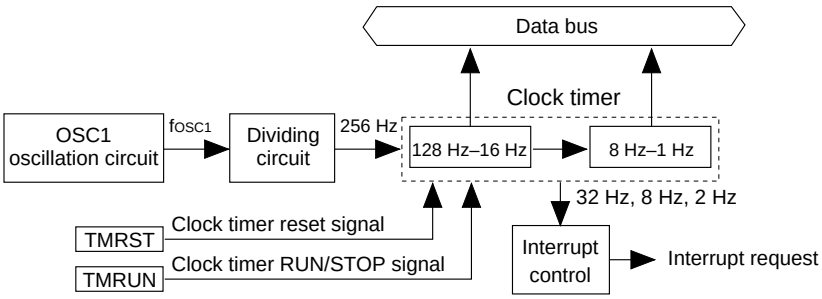


Fig. 4.8.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

4.8.2 Data reading and hold function

The 8 bits timer data are allocated to the address C9H and CAH.

C9H	D0: TM0 (128 Hz)	D1: TM1 (64 Hz)	D2: TM2 (32 Hz)	D3: TM3 (16 Hz)
CAH	D0: TM4 (8 Hz)	D1: TM5 (4 Hz)	D2: TM6 (2 Hz)	D3: TM7 (1 Hz)

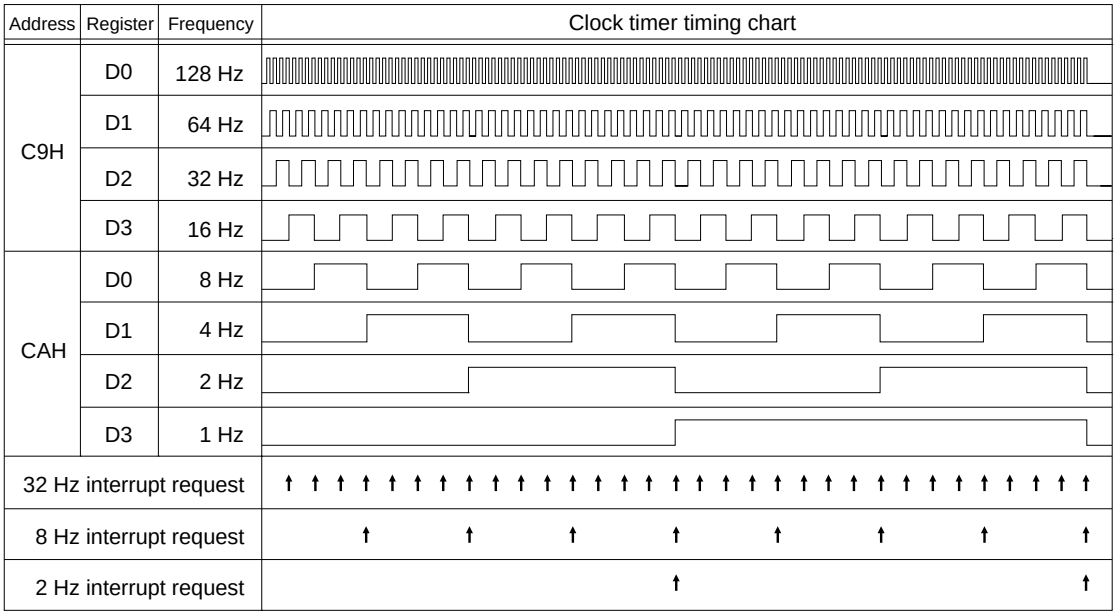
Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as 0FH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the S1C62920 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (varies due to the timing of the reading)

Note: When the high-order data has previously been read, since the low-order data is not held, you should be sure to first read from the low-order data.

4.8.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz and 2 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.8.3.1 is the timing chart of the clock timer.



(When fOSC1 = 32.768 kHz)

Fig. 4.8.3.1 Timing chart of clock timer

As shown in Figure 4.8.3.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.8.4 Control of clock timer

Table 4.8.4.1 shows the clock timer control bits and their addresses.

Table 4.8.4.1 Control bits of clock timer

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C8H	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST*5	Reset	Reset	–	Clock timer reset
C9H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
CAH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F4H	0	EIT2	EIT1	EIT0	0 *5	– *2			Unused
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R	R/W			EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FCH	0	IT2	IT1	IT0	0 *5	– *2			Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

TM0–TM7: Timer data (C9H, CAH)

The 128 Hz–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.
By reading the low-order data (C9H), the high-order data (CAH) is held while the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (varies due to the timing of the reading)

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (C8H•D0)

This bit resets the clock timer.

When "1" is written:	Clock timer reset
When "0" is written:	No operation
Reading:	Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP (C8H•D1)

This bit controls RUN / STOP of the clock timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The clock timer enters the RUN status when "1" is written to TMRUN, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, this register is set to "0".

EIT0, EIT1, EIT2: Interrupt mask registers (F4H•D0, D1, D2)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

The interrupt mask registers (EIT0, EIT1, EIT2) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz).
At initial reset, these registers are all set to "0".

IT0, IT1, IT2: Interrupt factor flags (FCH•D0, D1, D2)

These flags indicate the status of the clock timer interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags (IT0, IT1, IT2) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags can be reset through being read out by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
At initial reset, these flags are set to "0".

4.8.5 Programming notes

(1) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

4.9 Serial Interface (SIN, SOUT, $\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$)

4.9.1 Configuration of serial interface

The S1C62920 has a synchronous clock type 8 bits serial interface built-in.
The configuration of the serial interface is shown in Figure 4.9.1.1.
The CPU, via the 8 bits shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8 bits shift register, it can convert parallel data to serial data and output it to the SOUT terminal. The $\overline{\text{SCLK}}$ terminal outputs or inputs synchronous clock. When this serial interface is used in master mode (internal clock mode: when the S1C62920 is to be the master for serial input/output), FOUT frequency that is selected by the mask option is used for the synchronous clock, and the clock is output from the $\overline{\text{SCLK}}$ terminal. When this serial interface is used in slave mode (external clock mode: when the S1C62920 is to be the slave for serial input/output), input the synchronous clock to the $\overline{\text{SCLK}}$ terminal from a master device. Also, when the serial interface is used in slave mode, $\overline{\text{SRDY}}$ signal which indicates whether or not the serial interface is available to transmit or receive can be output to the $\overline{\text{SRDY}}$ terminal.

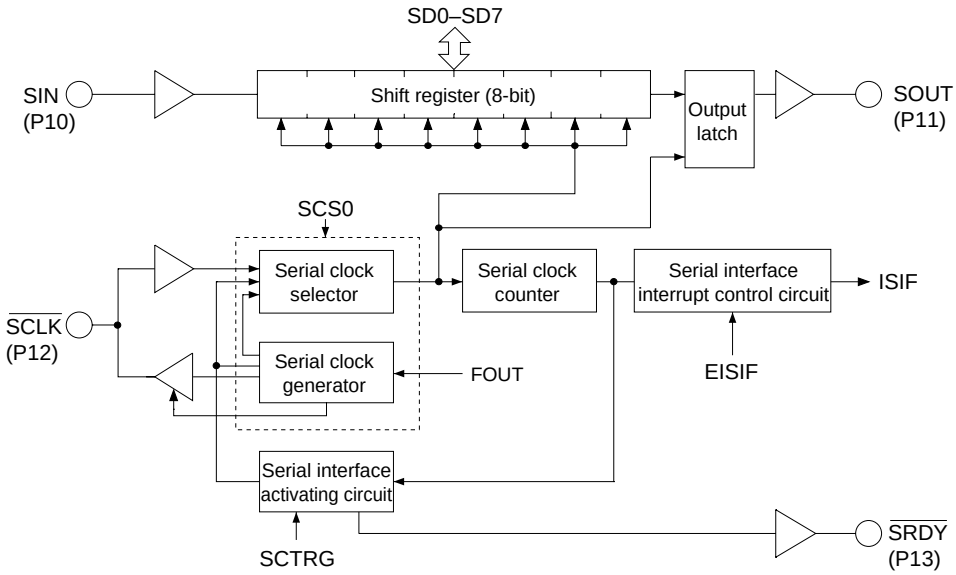


Fig. 4.9.1.1 Configuration of serial interface

The input/output ports of the serial interface are common used with the I/O ports P10–P13, and function of these ports can be selected through the software.
P10–P13 terminals and serial input/output correspondence are as follows:

Master mode	***Slave mode***
P10 = SIN (I)	P10 = SIN (I)
P11 = SOUT (O)	P11 = SOUT (O)
P12 = $\overline{\text{SCLK}}$ (O)	P12 = $\overline{\text{SCLK}}$ (I)
P13 = I/O port (I/O)	P13 = $\overline{\text{SRDY}}$ (O)

Note: At initial reset, P10–P13 are set to I/O ports.
When using the serial interface, switch the function (ESIF = "1") in the initial routine.

4.9.2 Master mode and slave mode of serial interface

The serial interface of the S1C62920 has two types of operation mode: master mode and slave mode.
In the master mode, it uses an internal (FOUT) clock as synchronous clock of the built-in shift register, generates this internal (FOUT) clock at the $\overline{SCLK}$ (P12) terminal and controls the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the $\overline{SCLK}$ (P12) terminal and uses it as the synchronous clock to the built-in shift register.
The master mode and slave mode are selected by writing data to SCS0 register. Writing "1" to the SCS0 register sets the serial interface into the master mode, and writing "0" sets into the slave mode.

When the serial interface is set in the master mode, the FOUT clock selected by the mask option is used as the synchronous clock. It can be selected from among 4 types; OSC1, OSC1 /8, OSC1 /64 and OSC3.

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8 bits serial data, is controlled as follows:

- At master mode, after output of 8 clocks from the $\overline{SCLK}$ (P12) terminal, clock output is automatically suspended and $\overline{SCLK}$ (P12) terminal is fixed at high level.
- At slave mode, after input of 8 clocks to the $\overline{SCLK}$ (P12) terminal, subsequent clock inputs are masked.

A sample basic serial input/output portion connection is shown in Figure 4.9.2.1.

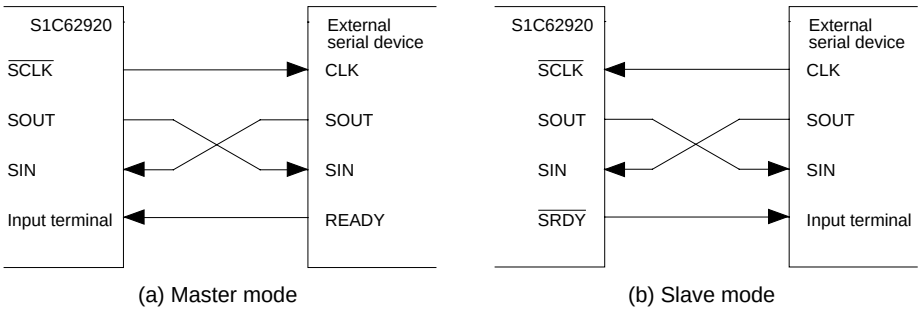


Fig. 4.9.2.1 Sample basic connection of serial input/output section

4.9.3 Data input/output and interrupt function

The serial interface of S1C62920 can input/output data via the internal 8 bits shift register. The shift register operates by synchronizing with either the synchronous clock output from $\overline{SCLK}$ (P12) terminal (master mode), or the synchronous clock input to $\overline{SCLK}$ (P12) terminal (slave mode).
The serial interface generates interrupt on completion of the 8 bits serial data input/output. Detection of serial data input/output is done by the counting of the synchronous clock $\overline{SCLK}$; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates interrupt.
The serial data input/output procedure data is explained below:

(1) Serial data output procedure and interrupt

The S1C62920 serial interface is capable of output parallel data as serial data, in units of 8 bits.
By setting the parallel data to 4 bits registers SD0–SD3 (E9H) and SD4–SD7 (EAH) individually and writing "1" to SCTRG bit (E8H•D1), it synchronizes with the synchronous clock and serial data is output at the SOUT (P11) terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{SCLK}$ (P12) terminal while in the slave mode, external clock which is input from the $\overline{SCLK}$ (P12) terminal. The serial data output from the built-in shift register is shifted with the falling edge of the $\overline{SCLK}$ signal.

When the output of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIF (F8H • D0) is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF (F0H • D0). Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after output of the 8 bits data.

(2) Serial data input procedure and interrupt

The S1C62920 serial interface is capable of inputting serial data as parallel data, in units of 8 bits.
The serial data is input from the SIN (P10) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8 bits shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{\text{SCLK}}$ (P12) terminal while in the slave mode, external clock which is input from the $\overline{\text{SCLK}}$ (P12) terminal.
The serial data to the built-in shift register is read with the rising edge of the $\overline{\text{SCLK}}$ signal. Moreover, the shift register is sequentially shifted as the data is fetched.

When the input of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after input of the 8 bits data.

The data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

In the S1C62920, the input / output permutation of serial data is fixed at LSB first.

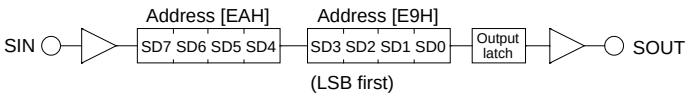


Fig. 4.9.3.1 Serial data input/output permutation

(4) $\overline{\text{SRDY}}$ signal

When the S1C62920 serial interface is used in the slave mode (external clock mode), $\overline{\text{SRDY}}$ is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. $\overline{\text{SRDY}}$ signal is output from $\overline{\text{SRDY}}$ (P13) terminal.
$\overline{\text{SRDY}}$ signal becomes "0" (low) when the S1C62920 serial interface becomes available to transmit or receive data; normally, it is at "1" (high).
$\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to $\overline{\text{SCLK}}$ (P12) terminal (i.e., when the serial input / output begins transmitting or receiving data). Moreover, when data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".

(5) Timing chart

The S1C62920 serial interface timing chart is shown in Figure 4.9.3.2.

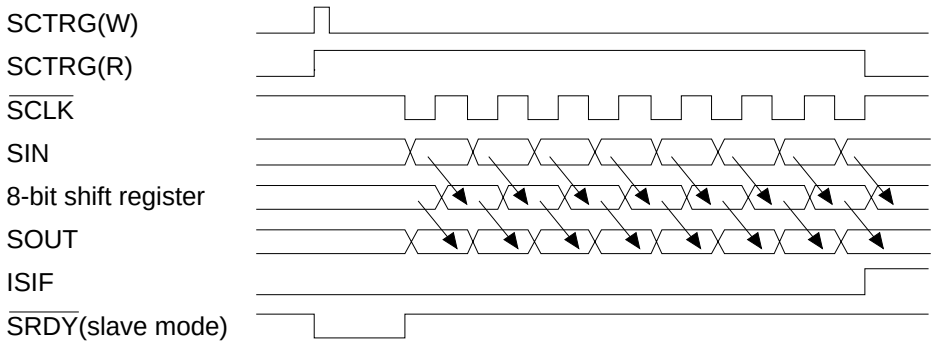


Fig. 4.9.3.2 Serial interface timing chart

4.9.4 Mask option

Since the input/output terminal of the serial interface is dual used with the I/O ports (P10–P13), the mask option that selects the specification for the I/O port is also applied to the serial interface.

(1) Output specification

The output specification of the terminals SOUT, $\overline{\text{SCLK}}$ (during the master mode) and $\overline{\text{SRDY}}$ (during the slave mode) that is used as output in the input/output port of the serial interface is respectively selected by the mask options of P11, P12 and P13.
Either complementary output or N channel (Nch) open drain as output specification may be selected. However, even if Nch open drain has been selected, application on the terminal of voltage exceeding power source voltage is not permitted.

(2) Pull up resistor

Whether or not the SIN (P10) terminal and $\overline{\text{SCLK}}$ (P02) terminal (during slave mode) will use built-in pull up resistor can be selected.
Normally, the use of pull up resistor should be selected.

(3) FOUT frequency

The FOUT frequency, which is selected by the mask option to select the output port R02 special output specification, is used for the synchronous clock. When the serial interface is used, the FOUT frequency must be selected even if the R02 port is not used as the FOUT output.
It can be selected from the four types listed below.

1. OSC1 2. OSC1 /8 3. OSC1 /64 4. OSC3

4.9.5 Control of serial interface

Table 4.9.5.1 list the serial interface control bits and their addresses.

Table 4.9.5.1 Control bits of serial interface

address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E8H	SCS0	0	SCTRG	ESIF	SCS0	0	FOUT	Slave	Serial I/F clock mode selection
					0 *5	– *2			Unused
					SCTRG(W)	– *2	Trigger	–	Serial I/F clock trigger (writing)
	R/W	R	R/W		SCTRG(R)	0	Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF port	I/O port	P1 port function selection
E9H	SD3	SD2	SD1	SD0	SD3	– *2			MSB
					SD2	– *2			Serial I/F data (low-order 4 bits)
	R/W				SD1	– *2			
					SD0	– *2			LSB
EAH	SD7	SD6	SD5	SD4	SD7	– *2			MSB
					SD6	– *2			Serial I/F data (high-order 4 bits)
	R/W				SD5	– *2			
					SD4	– *2			LSB
F0H	0	0	0	EISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
F8H	0	0	0	ISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ISIF *4	0	Yes	No	Interrupt factor flag (Serial I/F)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

ESIF: Serial interface enable (E8H•D0)

Sets P10–P13 to the input/output port for the serial interface.

When "1" is written:	Serial interface
When "0" is written:	I/O port
Reading:	Valid

The ESIF is the serial interface enable register and P10–P13 terminals become serial input/output terminals (SIN, SOUT, $\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$) when "1" is written, and they become I/O port terminals when "0" is written. The P13 terminal functions as $\overline{\text{SRDY}}$ output terminal only in the slave mode, and in the master mode, it functions as the I/O port terminal.
At initial reset, this register is set to "0".

SCS0: Clock mode selection (E8H•D3)

Selects the clock mode for the serial interface.

When "1" is written:	Master mode (FOUT clock is used)
When "0" is written:	Slave mode (external clock is used)
Reading:	Valid

When "1" is written to SCS0, the serial interface enters in the master mode. When "0" is written, it enters in the slave mode.
For the synchronous clock that is used in the master mode, the FOUT clock, witch is selected as a R02 special output specification and FOUT frequency by the mask option, is used. Therefore, the FOUT frequency should be selected even if the R02 port is not used as a special output (FOUT output).
At initial reset, this register is set to "0".

SCTRG: Clock trigger/status (E8H•D1)

This is a trigger to start input/output of synchronous clock ($\overline{\text{SCLK}}$).

• ***During writing operation***

When "1" is written:	Trigger
When "0" is written:	No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock ($\overline{\text{SCLK}}$) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.)
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

• ***During reading operation***

When "1" is read:	RUN status
When "0" is read:	STOP status
Writing:	Invalid

When read out this bit, it indicates the status of serial interface clock.
After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation.
When the synchronous clock input/output is completed, this latch is reset to "0".
At initial reset, this register is set to "0".

SD0–SD3, SD4–SD7: Serial interface data register (E9H, EAH)

These registers are used for writing and reading serial data.

• ***During writing operation***

When "1" is written:	High level
When "0" is written:	Low level

Writes serial data will be output to SOUT (P11) terminal. From the SOUT (P11) terminal, the data converted to serial data as high (V_{DD}) level bit for bits set at "1" and as low (V_{SS}) level bit for bits set at "0".

• ***During reading operation***

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN (P10) terminal can be read by this register.
The data converted to parallel data, as high (V_{DD}) level bit "1" and as low (V_{SS}) level bit "0" input from SIN (P10) terminal. Perform data reading only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers will be undefined.

EISIF: Interrupt mask register (F0H•D0)

This is the interrupt mask register of the serial interface.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With this register, masking of the serial interface interrupt can be selected.
At initial reset, this register is set to "0".

ISIF: Interrupt factor flag (F8H•D0)

This is the interrupt factor flag of the serial interface.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
The interrupt factor flag is reset when it has been read out.
Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8 bits data input/output.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
At initial reset, this flag is set to "0".

4.9.6 Programming notes

(1) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (SCTRG = "0").

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

(3) When using the serial interface in the master mode and FOUT frequency is set to OSC3, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting the serial input/output, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time. (refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

(4) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.10 R/F Converter

4.10.1 Configuration of R/F converter

The S1C62920 has CR oscillation type R/F converter.
Three systems (three sensor connection terminals: SEN0, SEN1, SEN2) of CR oscillation circuit are built into this R/F converter, so it is possible to compose three types of R/F conversion circuits by connecting different resistive sensors to each CR oscillation circuit.
Each of the R/F conversion circuits uses the same CR oscillation circuit and the same external reference resistance. The R/F conversion circuit to be used is selected by the software.
Resistance value (relative value to external reference resistance) of the resistive sensor that has been connected to the sensor input terminal is converted into frequency by the CR oscillation circuit and the number of clocks is counted in the built-in measurement counter. By reading the value of the measurement counter, it can obtain the data after digitally-converting the value detected by the sensor.
Various sensor circuits such as temperature measurement circuits using a thermistor can be easily realized using this R/F converter.
The configuration of the R/F converter is shown in Figure 4.10.1.1.

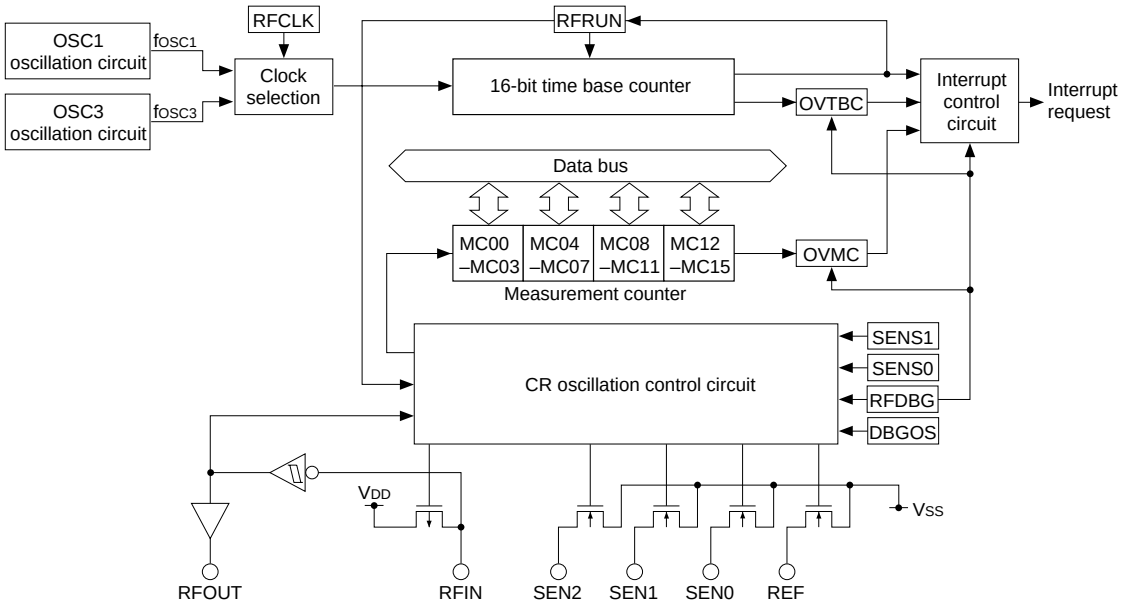


Fig. 4.10.1.1 Configuration of R/F converter

4.10.2 Connection terminals and CR oscillation circuit

The S1C62920 has the connecting terminals for one reference resistance and three sensors so that three R/F converters can be configured.
Figure 4.10.2.1 shows the connection diagram of external elements.

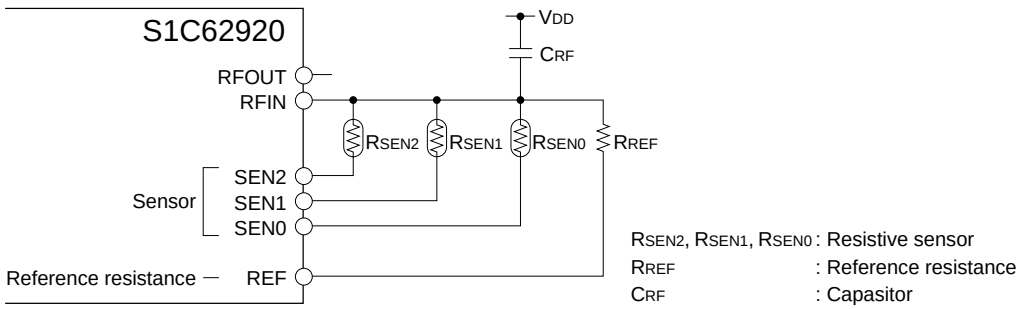


Fig. 4.10.2.1 R/F converter external connection diagram

The capacitor for the CR oscillation circuit is commonly used for the reference resistance and both sensors. The CR oscillation circuit is configured with the reference resistance, each of the sensors and this capacitor and can R/F-convert using the reference resistance and the sensor selected by the software.
The R/F converter performs CR oscillation using each of the two resistances (sensor and reference resistance) in the same period, and counts the CR oscillation clock. Difference in counted oscillation frequency can be evaluated in terms of the difference between the respective resistance values. Measurement results can be obtained from the changes in resistance values after correcting the difference according to the program. Consequently, a resistance that has a resistance value equivalent to the middle of the measurement range of the sensor to be used for measurement should be used as a reference resistance. An element that does not change due to temperature or other environmental conditions must be used as the reference resistance.

Sensor to be R/F-converted can be selected as below using the registers SENS0 and SENS1.

SENS1 = "1", SENS0 = X ... SEN2 is selected
SENS1 = "0", SENS0 = "1" ... SEN1 is selected
SENS1 = "0", SENS0 = "0" ... SEN0 is selected

The following explains the operation of the CR oscillation circuit that is configured with the above connection.

The operation of the CR oscillation circuit is similar for both reference resistance and sensors, so the following explanation is in the case of the CR oscillation circuit with the sensor connected to the SEN0 terminal.
Figure 4.10.2.2 shows the CR oscillation circuit configured with the SEN0 terminal.

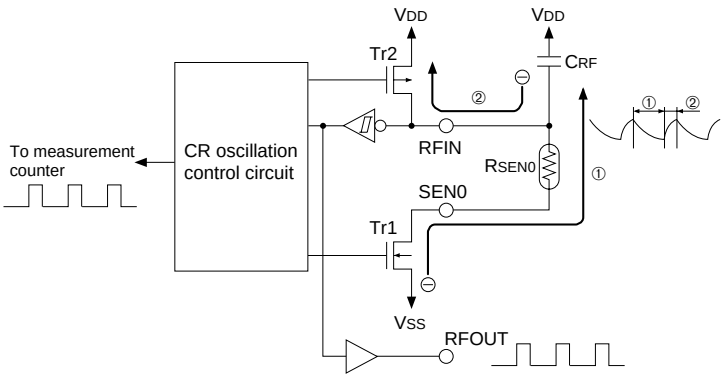


Fig. 4.10.2.2 CR oscillation circuit

The Tr1 turns on first, and the capacitor (C_{RF}) connected between the V_{DD} and RFIN terminals is charged through the sensor (R_{SEN0}). If the voltage level of the RFIN terminal decreases, the Tr1 turns off and the Tr2 turns on. As a result, the capacitor becomes discharged, and oscillation is performed according to CR time constant. The time constant changes as the sensor resistance value fluctuates, producing a difference from the oscillation frequency of the reference resistance.

The above example is in the case of a SEN0 terminal. Controlling whether the reference resistance or the sensor selected by the software to be CR-oscillated (controlling a transistor of terminal) is done by the CR oscillation circuit.

Oscillation waveforms are shaped by the schmitt trigger and transmitted to the measurement counter. The clock transmitted to the counter is also output from the RFOUT terminal. As a result, oscillation frequency can be identified by the oscilloscope. Since this monitor has no effect on oscillation frequency, it can be used to adjust CR oscillation frequency.
Oscillation waveforms and waveforms output from the RFOUT terminal are shown in Figure 4.10.2.3.

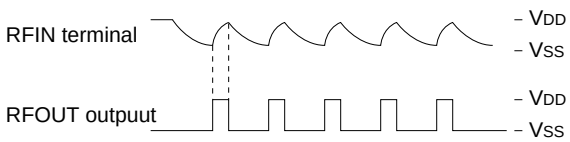


Fig. 4.10.2.3 Oscillation waveform

4.10.3 Operation of R/F conversion

(1) Counter

The R/F converter incorporates two types of counters. One is the measurement counter MCxx that counts the aforementioned oscillation clock, and the other is the time base counter that counts the internal clock for reference counting.

The measurement counter is used to count (count up) the CR oscillation clock by the reference resistance and sensor, and the results of R/F conversion can be obtained by reading this counter. The measurement counter is 16 bits (MC00–MC15) and can be read in 4-bit units.
This counter is designed so that it counts serially in order of the reference resistance and the sensor. Also it switches the CR oscillation from reference resistance to sensor at the point an overflow occurs (counter = 0000H) during counting of the reference resistance oscillation. Furthermore, both of the oscillation times of the reference resistance and sensor are designed to be the same by the time base counter described later. Therefore, by converting a proper initial value for counting of the oscillation of the reference resistance into a complement (value subtracted from 0000H) and setting it into the counter before starting to count, the number of counts for the sensor oscillation is obtained by reading this counter after the R/F conversion. In other words, the difference between the reference resistance and sensor oscillation frequencies can be found easily. For instance, if resistance values of the reference resistance and the sensor are equivalent, the same value as the initial value before converting into a complement will be obtained as the result.

The time base counter is a 16-bit up/down counter to equal both oscillation times for the reference resistance and the sensor. For the input clock, either OSC1 clock (Typ. 32.768 kHz) or OSC3 clock can be selected using the software. This selection can be done using the register RFCLK (D0H•D1). When "1" is set to the register, OSC3 clock is selected and when "0" is set, OSC1 clock is selected.
When R/F conversion is started, the time base counter starts counting-down from "0000H" at the same time the measurement counter starts counting for oscillation by reference resistance. After that, when the oscillation switches to the sensor side, this counter also switches to counting-up and counts up oppositely from the value that is counted during oscillation of the reference resistance. The counting-up continues until the counter value is "0000H". When the counter becomes "0000H", the counter stops and the sensor oscillation also stops. In other words, the oscillation times of reference resistance and sensor can be made the same.

(2) R/F conversion sequence

R/F conversion starts by writing "1" to the register RFRUN (D2H•D1).
Further the following settings must be done before starting the R/F conversion.

1. Sensor selection (SENS0, SENS1)
2. Selecting the time base counter input clock (RFCLK)
3. Initial value setting to the measurement counter
4. Turning the OSC3 oscillation ON (OSCC) ...when the OSC3 clock is selected at 2.

Note: It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting a remote output, secure 5 msec or more waiting time for oscillation stabilization after turning the OSC3 oscillation ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the waiting time.

When R/F conversion is initiated by the RFRUN register, oscillation by the reference resistance begins first, and the measurement counter starts counting up from the initial value by the oscillation clock. The time base counter also starts counting down by the internal clock.
Timing in starting oscillation and starting counting are shown in Figure 4.10.3.1.
CR oscillation starts in synchronizing with the falling edge of the OSC1 or OSC3 clock (one of these that is selected as the time base counter input clock) immediately after writing "1" to the RFRUN register.
The measurement counter starts counting up at the falling edge of the first clock after CR oscillation is initiated.
The time base counter becomes enable at the falling edge of the first internal clock (OSC1 or OSC3). Then, it counts down by the falling edge of the internal clock.

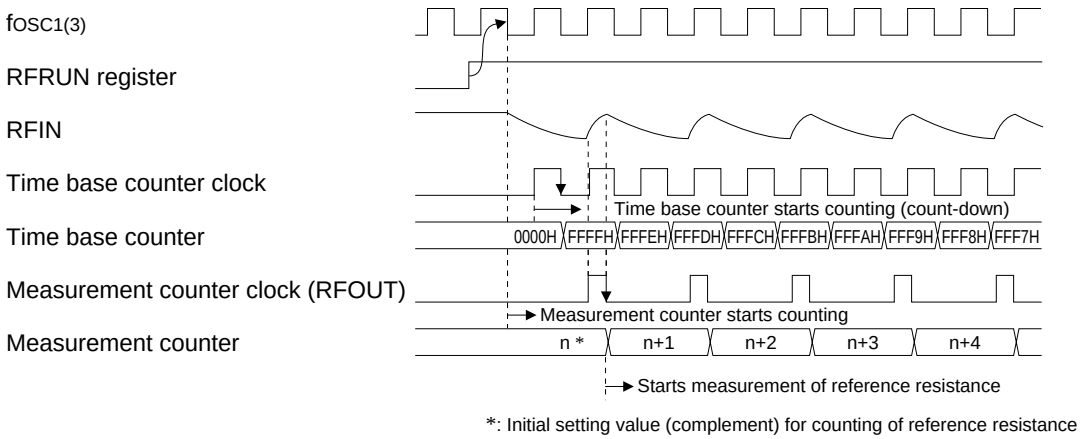


Fig. 4.10.3.1 Counting up start timing

If the measurement counter becomes "0000H" due to overflow, the oscillation is switched from the reference resistance side to the sensor side, and the measurement counter starts counting up according to the oscillation clock on the sensor side.
The time base counter shifts to the counting-up mode at this point and starts counting up from the value that has been counted while the reference resistance was oscillating.
Timing in switching oscillation is shown in Figure 4.10.3.2.
The sensor oscillation starts in synchronization with the counting of the time base counter after a measurement of the reference resistance has completed.

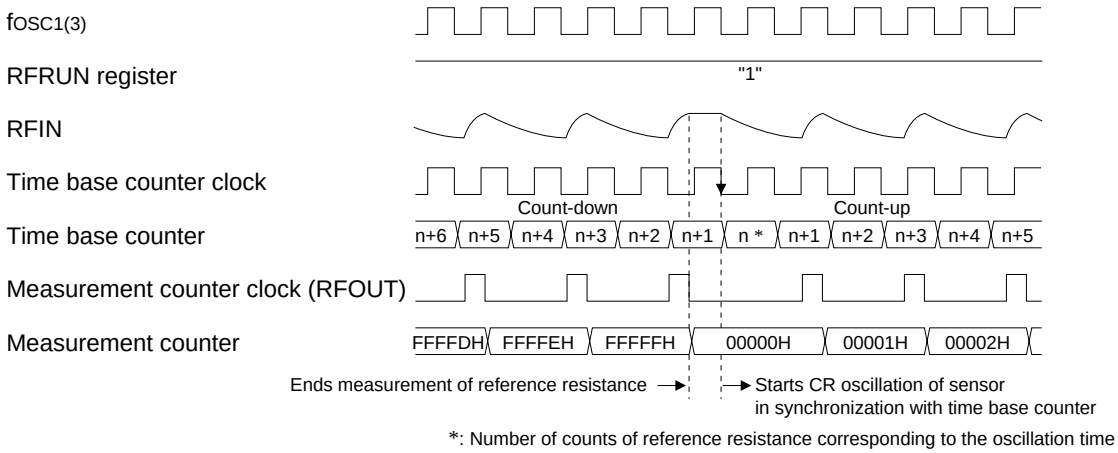


Fig. 4.10.3.2 Oscillation switch timing

When the time base counter has counted up to "0000H", the counting operation of both counters and CR oscillation stop, and an interrupt occurs. At the same time, the RFRUN register is set to "0", and the R/F converter circuit stops operation completely.
Figure 4.10.3.3 shows the R/F conversion end timing.
To prevent malfunction of the measurement counter, a CR oscillation clock is also counted in the measurement counter when the time base counter becomes "0000H". An interrupt occurs in synchronizing with the rising edge of OSC1 or OSC3 (one of these selected as the time base counter input clock) immediately after the measurement counter stops.
Further, the timing of the RFRUN register when it is set to "0" is the falling edge of the interrupt request signal.

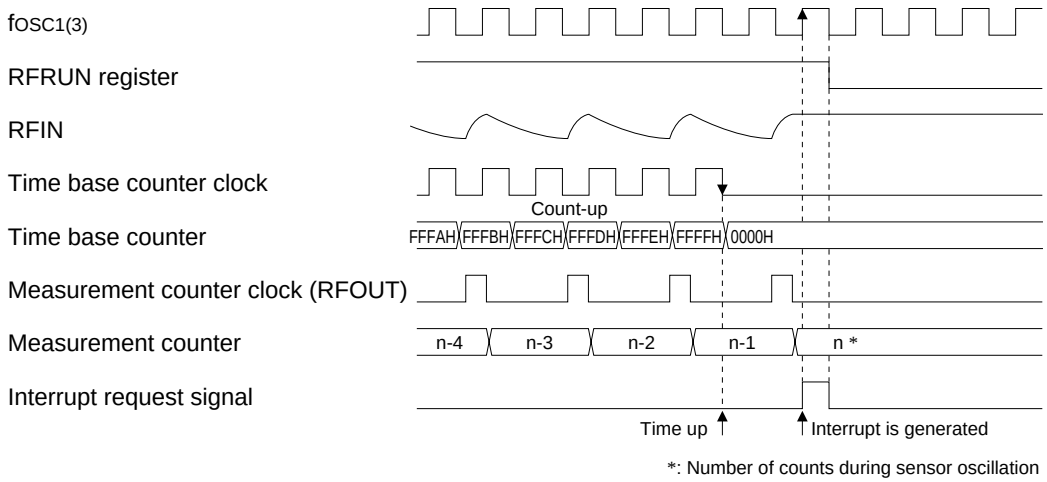


Fig. 4.10.3.3 R/F conversion end timing

By the above operation, the sensor is oscillated for the same period of time as the reference resistance is oscillated. Therefore, the difference in oscillation frequency can be measured from the values counted by the measurement counter.

Since the reference resistance is oscillated until the measurement counter overflows, an appropriate initial value needs to be set before R/F conversion is started. If a smaller initial value is set, a longer counting period is possible, thereby ensuring more accurate detection. However, the time base counter may overflow while counting the oscillation frequency of the reference resistance.
If an overflow occurs, CR oscillation and R/F conversion is terminated immediately. Also in such cases, interrupt occurs. Moreover, the measurement counter may overflow while counting the sensor oscillation depending on initial value setting. If the measurement counter overflows, CR oscillation and R/F conversion is terminated at that point and an interrupt occurs.
When these overflows occur, the correct value cannot be read. Therefore, the overflow flags are provided to judge whether the read data is correct or an overflow occurs. There are two overflow flags; OVMC (D2H•D2) that indicates an measurement counter overflow and OVTBC (D2H•D3) that indicates an time base counter overflow. These flags are set to "1" if respective counter overflows. These flags are reset to "0" when R/F conversion is started or when "1" is written to the flag. When the interrupt occurs, be sure to read the overflow flags and check overflow.
The initial value to be set depends on the measurable range by the sensor or where to set the reference resistance value within that range.
The initial value must be set taking the above into consideration.

Convert the initial value into a complement (value subtracted from 0000H) before setting it on the measurement counter. Since the data output from the measurement counter after R/F conversion matches data detected by the sensor, process the difference between that value and the initial value before it is converted into a complement according to the program and calculate the target value.

The above operations are shown in Figure 4.10.3.4.

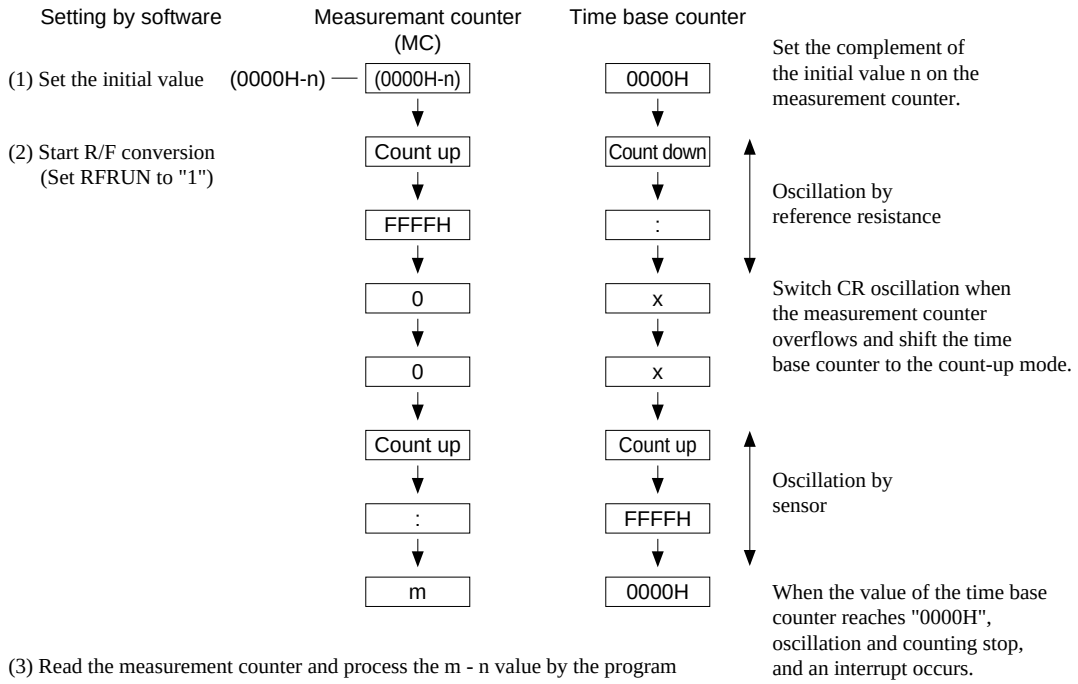


Fig. 4.10.3.4 Sequence of R/F conversion

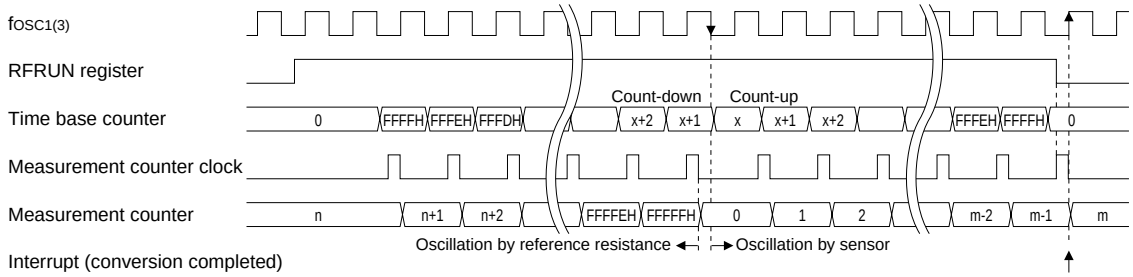
Note: Set the initial value of the measurement counter taking into account the measurable range and the overflow of counters.

(3) Operation mode

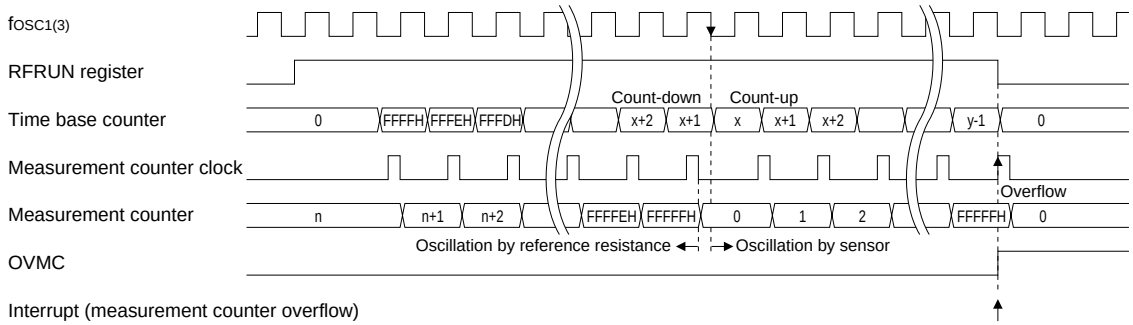
Thus far we explained the R/F converter to be operated in the normal mode.
The debug mode is set as an operating mode for the R/F converter in addition to the normal mode, and can be set by writing "1" to the register RFDBG (D0H•D2). To return to the normal mode, write "0" to the RFDBG.
The debug mode is provided for hardware/software debugging. It functions to continuously oscillate only the reference resistance side or sensor side. This function can measure the oscillation frequency by the resisters connected to each terminal. (Overflow of each counter and interrupt do not occur.) Sensor selection function is valid even in the debug mode. The oscillating operation starts by writing "1" to the RFRUN and is continued until "0" is written to the RFRUN.
Whether to oscillate the reference resistance or sensor is selected using the register DBGOS (D0H•D3). When "1" is written to the DBGOS register, the sensor side is selected. When "0" is written, the reference resister side is selected. This setting is valid only in the debug mode.

4.10.4 Interrupt function

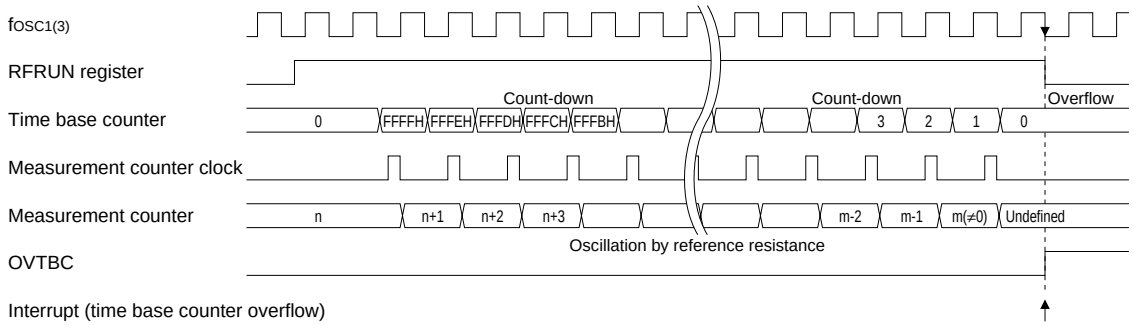
The R/F converter has a function which allows interrupt to occur after R/F conversion.
When the time base counter is counted up to "0000H", both counters stop counting. The interrupt factor flag IRF (F9H•D0) is set to "1" at the rising edge of the next clock (OSC1 or OSC3 clock that has been selected as the time base counter input clock).
If the time base counter overflows during counting of the reference resistance oscillation, or the measurement counter overflows during counting of the sensor oscillation, the interrupt factor flag IRF is also set to "1".
This interrupt factor allows masking by the interrupt mask register EIRF (F1H•D0). When the EIRF has been set at "1", an interrupt occurs in the CPU. When the EIRF is set at "0", no interrupt will occur in the CPU even if the interrupt factor flag is set to "1".
The interrupt factor flag is reset to "0" by reading.
Timing of interrupt by the R/F converter is shown in Figure 4.10.4.1.



(1) Completion interrupt



(2) Measurement counter overflow



(3) Time base counter overflow

Fig. 4.10.4.1 Timing of R/F converter interrupt

Note:
- *When the R/F converter interrupt is generated, be sure to check whether or not the R/F conversion has completed normally by reading the overflow flags.*
- *When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/F converter interrupt occurs.*
- *Reading of interrupt factor flag is available at EI, but be careful in the following cases.*
  If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.10.5 Control of R/F converter

Table 4.10.5.1 lists the control bits and their addresses for the R/F converter.

Table 4.10.5.1 Control bits of R/F converter

Address *7	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
D0H	DBGOS	RFDBG	RFCLK	0	DBGOS	0	Sensor	Ref.-R	R/F converter debugging element selection
					RFDBG	0	Debug	Normal	R/F converter debug mode selection
	R/W			R	RFCLK	0	OSC3	OSC1	R/F converter clock source selection
					0	– *2			Unused
D1H	0	0	SENS1	SENS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		SENS1	0			R/F converter sensor selection
					SENS0	0			0=SEN0, 1=SEN1, 2&3=SEN2
D2H	OVTBC	OVMC	RFRUN	0	OVTBC	0	Overflow	Non-ov	Time base counter overflow flag *6
					OVMC	0	Overflow	Non-ov	Measurement counter overflow flag *6
	R/W			R	RFRUN	0	Run	Stop	R/F converter Run/Stop
					0 *5	– *2			Unused
D3H	MC03	MC02	MC01	MC00	MC03	– *3			Measurement counter MC00–MC03
					MC02	– *3			
	R/W				MC01	– *3			
					MC00	– *3			
D4H	MC07	MC06	MC05	MC04	MC07	– *3			Measurement counter MC04–MC07
					MC06	– *3			
	R/W				MC05	– *3			
					MC04	– *3			
D5H	MC11	MC10	MC09	MC08	MC11	– *3			Measurement counter MC08–MC11
					MC10	– *3			
	R/W				MC09	– *3			
					MC08	– *3			
D6H	MC15	MC14	MC13	MC12	MC15	– *3			Measurement counter MC12–MC15
					MC14	– *3			
	R/W				MC13	– *3			
					MC12	– *3			
F1H	0	0	0	EIRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIRF	0	Enable	Mask	Interrupt mask register (R/F converter)
F9H	0	0	0	IRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IRF *4	0	Yes	No	Interrupt factor flag (R/F converter)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

DBGOS: Debugging element selection (D0H•D3)

Selects an element to be oscillated during the debug mode.

When "1" is written: Sensor
When "0" is written: Reference resistance
Reading: Valid

When "1" is written to DBGOS, sensor is continuously oscillated during the debug mode, and when "0" is written, reference resistance is continuously oscillated. This selection is valid only in the debug mode.
At initial reset, this register is set to "0".

RFDBG: Debug mode selection (D0H•D2)

Selects the debug mode of the R/F converter.

When "1" is written: Debug mode
When "0" is written: Normal mode
Reading: Valid

When "1" is written to RFDBG, the debug mode is selected, and when "0" is written, the normal mode is selected. When the debug mode is set, the oscillating operation of the element side selected by the DBGOS register can be done continuously.
At initial reset, this register is set to "0".

RFCLK: Input clock selection (D0H•D1)

Select an input clock of the time base counter.

When "1" is written: OSC3
When "0" is written: OSC1
Reading: Valid

When "1" is written to RFCLK, the OSC3 clock is selected. When "0" is written, the OSC1 clock (Typ. 32.768 kHz) is selected.
The initial value must be set on the measurement counter so that the time base counter will not overflow while CR oscillation is being counted.
At initial reset, these registers are set to "0".

SENS0, SENS1: Sensor selection (D1H•D0, D1)

Selects a sensor to be R/F-converted.

Table 4.10.5.2 Sensor selection

SENS1	SENS0	Sensor selected
1	X	SEN2
0	1	SEN1
0	0	SEN0

At initial reset, this register is set to "0".

MC0–MC15: Measurement counter (D3H–D6H)

This counter counts up according to the CR oscillation clock. It permits writing and reading on a 4-bit basis. The complement of the number of clocks to be counted by the oscillation of the reference resistance, must be entered in this counter prior to R/F conversion.
If R/F conversion is initiated, the counter counts up from the set initial value, first according to the oscillation clock of the reference resistance. When the counter reaches "0000H" due to overflow, the oscillation of the reference resistance stops, and the sensor starts oscillating. The counter continues counting according to the sensor oscillation clock. Counting time during the CR oscillation of the reference resistance is calculated by the time base counter. The measurement counter stops counting when the same period of time elapses. Number of clocks counted by the sensor oscillation can be evaluated from the value indicated by the counter when it stops. Calculate the target value by processing the above counted number according to the program.
Measurable range and the overflow of the counter must be taken into account when setting an initial value to be entered prior to R/F conversion.
After an initial reset, data in this counter become indefinite.

RFRUN: R/F conversion RUN/STOP (D2H•D1)

Starts R/F conversion and indicates the operating (RUN/STOP) status.

When "1" is written: R/F conversion starts
When "0" is written: R/F conversion stops

When "1" is read: RUN status
When "0" is read: STOP status

When "1" is written to RFRUN, R/F conversion starts. The register remains at "1" during R/F conversion and is set to "0" when R/F conversion is terminated.
When "0" is written to RFRUN during R/F conversion, R/F conversion is paused.
This register is set to "0" at initial reset, when the time base counter or measurement counter overflows, or when measurement is finished.

OVMC: Measurement counter overflow flag (D2H•D2)

Indicates whether the measurement counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred

When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the sensor, OVMC is set to "1" and the interrupt occurs at the same time.
This flag is reset by writing "1" or starting R/F conversion.
At initial reset, this flag is set to "0".

OVTBC: Time base counter overflow flag (D2H•D3)

Indicates whether the time base counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred

When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the reference resistance, OVTBC is set to "1" and the interrupt occurs at the same time.
This flag is reset by writing "1" or starting R/F conversion.
At initial reset, this flag is set to "0".

EIRF: Interrupt mask register (F1H•D0)

Select whether to mask interrupt with the R/F converter.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

The R/F converter interrupt is permitted when "1" is written to EIRF. When "0" is written, interrupt is masked.
At initial reset, this register is set to "0".

IRF: Interrupt factor flag (F9H•D0)

This flag indicates the status of the R/F converter interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

IRF is set to "1" when R/F conversion is terminated, when the time base counter overflows while counting the oscillation of the reference resistance, or the measurement counter overflows while counting the oscillation of the sensor.
From the status of this flag, the software can decide whether an R/F converter interrupt has occurred.
Further this flag is set in the above timing regardless of the interrupt mask register setting.
This flag is reset when the software has read it.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
After an initial reset, this flag is set to "0".

4.10.6 Programming notes

(1) Depending on the initial value of the measurement counter (MC), the measurement counter (MC) or the time base counter may overflow while the CR oscillation clock is being counted. When setting the initial value, pay attention to CR oscillation frequency, its fluctuation range and the input clock frequency of the time base counter. If an overflow occurs, R/F conversion is terminated immediately. When the R/F conversion result (measurement counter value) is read, check the overflow flags (OVMC and OVTBC).

(2) When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/F converter interrupt occurs.

(3) When using the OSC3 clock as the time base counter input clock, the OSC3 oscillation circuit must be ON (OSCC = "1") before starting R/F conversion.
It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting a remote output, secure 5 msec or more waiting time for oscillation stabilization after turning the OSC3 oscillation ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the waiting time.

(4) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.11 SVD (Supply Voltage Detection) Circuit

4.11.1 Configuration of SVD circuit

The S1C62920 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON / OFF can be controlled by the software.
The criteria voltage for evaluating the supply voltage can be set to 2.4 V, 2.5 V, 2.6 V or 2.7 V by the mask option and whether the supply voltage is more or less it can be read as data by the software.
Figure 4.11.1.1 shows the configuration of the SVD circuit.

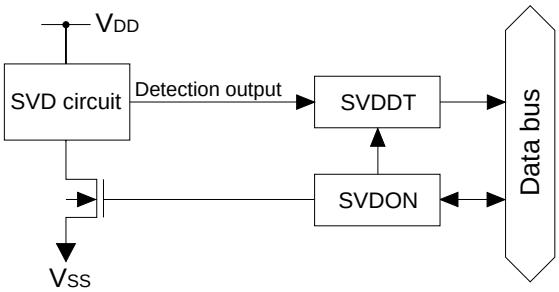


Fig. 4.11.1.1 Configuration of SVD circuit

4.11.2 SVD operation

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. The SVD circuit compares the criteria voltage and the supply voltage (V_{DD}–V_{SS}). As soon as SVDON is reset to "0", the result is loaded to in the SVDDT latch and SVD circuit goes OFF. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.

To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.
The detected data latched in SVDDT is maintained until the SVD circuit is operated again and a new detection result is latched.
When SVD is on, the IC draws a large current, so keep SVD off unless it is.

4.11.3 Control of SVD circuit

Table 4.11.3.1 shows the control bits and their addresses for the SVD circuit.

Table 4.11.3.1 Control bits for SVD circuit

Address *7	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
80H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	Supply voltage detection data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

SVDON: SVD circuit ON/OFF (80H•D0)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. As soon as SVDON is reset to "0", the result is loaded to in the SVDDT latch. To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec.
At initial reset, this register is set to "0".

SVDDT: SVD data (80H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

4.11.4 Programming notes

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.

(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

4.12 Interrupt and HALT

<Interrupt types>

The S1C62920 provides the following interrupt settings, each of which is maskable.

External interrupt:	• Input port interrupt	(1 system)
Internal interrupt:	• Clock timer interrupt	(3 systems)
	• Serial interface interrupt	(1 system)
	• R/F converter interrupt	(1 system)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.
Figure 4.12.1 shows the configuration of the interrupt circuit.

<HALT>

The S1C62920 has HALT function that considerably reduce the current consumption when it is not necessary.

The CPU enters the HALT status when the HALT instruction is executed.
In the HALT status, the operation of the CPU is stopped. However, the oscillation circuit operates. Reactivating the CPU from the HALT status is done by generating an interrupt request. When it does not reactivate upon an interrupt request, the watchdog timer will cause it to restart from the initial reset status.

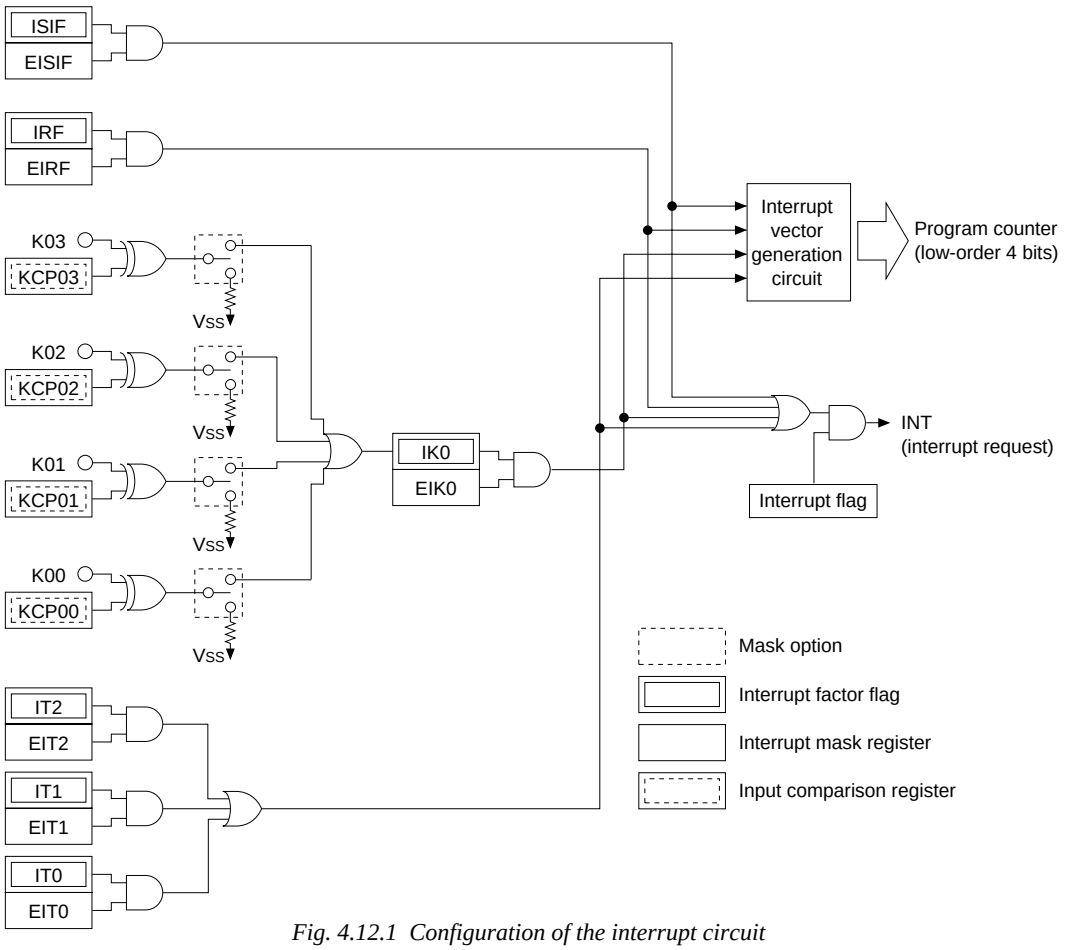


Fig. 4.12.1 Configuration of the interrupt circuit

4.12.1 Interrupt factor

Table 4.12.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when any of the conditions below set an interrupt factor flag to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read out.
At initial reset, the interrupt factor flags are reset to "0".

Table 4.12.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Serial interface (data send/receive has completed)	ISIF	(F8H•D0)
R/F converter (R/F conversion has completed)	IRF	(F9H•D0)
K00–K03 input (falling or rising edge)	IK0	(FBH•D0)
Clock timer 2 Hz (falling edge)	IT2	(FCH•D2)
Clock timer 8 Hz (falling edge)	IT1	(FCH•D1)
Clock timer 32 Hz (falling edge)	IT0	(FCH•D0)

Note: Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.12.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read / write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.12.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.12.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EISIF	(F0H•D0)	ISIF	(F8H•D0)
EIRF	(F1H•D0)	IRF	(F9H•D0)
EIK0	(F3H•D0)	IK0	(FBH•D0)
EIT2	(F4H•D2)	IT2	(FCH•D2)
EIT1	(F4H•D1)	IT1	(FCH•D1)
EIT0	(F4H•D0)	IT0	(FCH•D0)

4.12.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).
② The interrupt request causes the value of the interrupt vector (page 1, 02H–0AH) to be set in the program counter.
③ The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.12.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Note: The processing in ① and ② above take 12 cycles of the CPU system clock.

Table 4.12.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt request	Priority
102H	Serial interface	High
104H	R/F converter	↑
108H	K00–K03 input	↓
10AH	Clock timer	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.12.4 Control of interrupt

Table 4.12.4.1 shows the interrupt control bits and their addresses.

Table 4.12.4.1 Control bits of interrupt

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	Input comparison register (K00–K03)
	R/W				KCP02	1	↓	↑	
					KCP01	1	↓	↑	
					KCP00	1	↓	↑	
F0H	0	0	0	EISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
F1H	0	0	0	EIRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIRF	0	Enable	Mask	Interrupt mask register (R/F converter)
F3H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F4H	0	EIT2	EIT1	EIT0	0 *5	– *2			Unused
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R	R/W			EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
F8H	0	0	0	ISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ISIF *4	0	Yes	No	Interrupt factor flag (Serial I/F)
F9H	0	0	0	IRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IRF *4	0	Yes	No	Interrupt factor flag (R/F converter)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
FCH	0	IT2	IT1	IT0	0 *5	– *2			Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

EISIF: Interrupt mask register (F0H•D0)
ISIF: Interrupt factor flag (F8H•D0)

..... See Section 4.9, "Serial Interface".

EIRF: Interrupt mask register (F1H•D0)
IRF: Interrupt factor flag (F9H•D0)

..... See Section 4.10, "R/F Converter".

KCP03–KCP00: Input comparison registers (92H)
EIK0: Interrupt mask register (F3H•D0)
IK0: Interrupt factor flag (FBH•D0)

..... See Section 4.4, "Input Ports".

EIT2, EIT1, EIT0: Interrupt mask registers (F4H•D2–D0)
IT2, IT1, IT0: Interrupt factor flags (FCH•D2–D0)

..... See Section 4.8, "Clock Timer".

4.12.5 Programming notes

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The S1C62920 contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 5.1.1 Circuits and control registers

Circuit (and Item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
LCD power supply circuit	LPWR
SVD circuit	SVDON

See Chapter 7, "ELECTRICAL CHARACTERISTICS", for order of current consumption.

Below are the circuit statuses at initial reset.

CPU:	Operating status
CPU operating frequency:	Low speed side (CLKCHG = "0"), OSC3 oscillation circuit OFF status (OSCC = "0")
LCD power supply circuit:	OFF status (LPWR = "0")
SVD circuit:	OFF status (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Watchdog timer

When the watchdog timer is being used, the software must reset it within 3-second cycles.

Oscillation circuit

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

OSC1 → OSC3
1. Set OSCC to "1" (OSC3 oscillation ON)
2. Maintain 5 msec or more
3. Set CLKCHG to "1" (OSC1 → OSC3)

OSC3 → OSC1
1. Set CLKCHG to "0" (OSC3 → OSC1)
2. Set OSCC to "0" (OSC3 oscillation OFF)

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for turning the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) If it is not necessary to operate the CPU in high-speed and the OSC3 clock is not needed for some peripheral circuits, turn the OSC3 oscillation circuit off (CLKCHG = "0", OSCC = "0") to reduce current consumption.

Input ports

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times$ 1.6 [sec]
R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

(2) When the input comparison register (KCP00–KCP03) is set, the interrupt factor flag (IK0) may be set to "1" depending on the status of the input port terminal. Consequently, when setting this register, do it in the DI status (interrupt flag = "0") and then read the interrupt factor flag in order to reset.

Output ports

(1) When BZ and FOUT are selected, a hazard may be observed in the output waveform when the data of the output register changes.

(2) When selecting f_{OSC3} as the FOUT clock frequency, it is necessary to control the OSC3 oscillation circuit. See Section 4.3, "Oscillation Circuit" for details of the control.

I/O ports

When input terminals are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching data during input mode, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times$ 1.6 [sec]
R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

LCD driver

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) Since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

(3) 100 msec or more time is necessary for stabilizing the LCD drive voltages V_{C1} and V_{C3} after setting the LCD power control register LPWR to "1". Be careful of the segment-on right after the power is turned on.

Clock timer

(1) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

Serial interface

(1) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (SCTRG = "0").

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

(3) When using the serial interface in the master mode and FOUT frequency is set to OSC3, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting the serial input/output, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time. (refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

R/F converter

(1) Depending on the initial value of the measurement counter (MC), the measurement counter (MC) or the time base counter may overflow while the CR oscillation clock is being counted. When setting the initial value, pay attention to CR oscillation frequency, its fluctuation range and the input clock frequency of the time base counter. If an overflow occurs, R/F conversion is terminated immediately. When the R/F conversion result (measurement counter value) is read, check the overflow flags (OVMC and OVTBC).

(2) When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/F converter interrupt occurs.

(3) When using the OSC3 clock as the time base counter input clock, the OSC3 oscillation circuit must be ON (OSCC = "1") before starting R/F conversion.
It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting a remote output, secure 5 msec or more waiting time for oscillation stabilization after turning the OSC3 oscillation ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the waiting time.

SVD circuit

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.

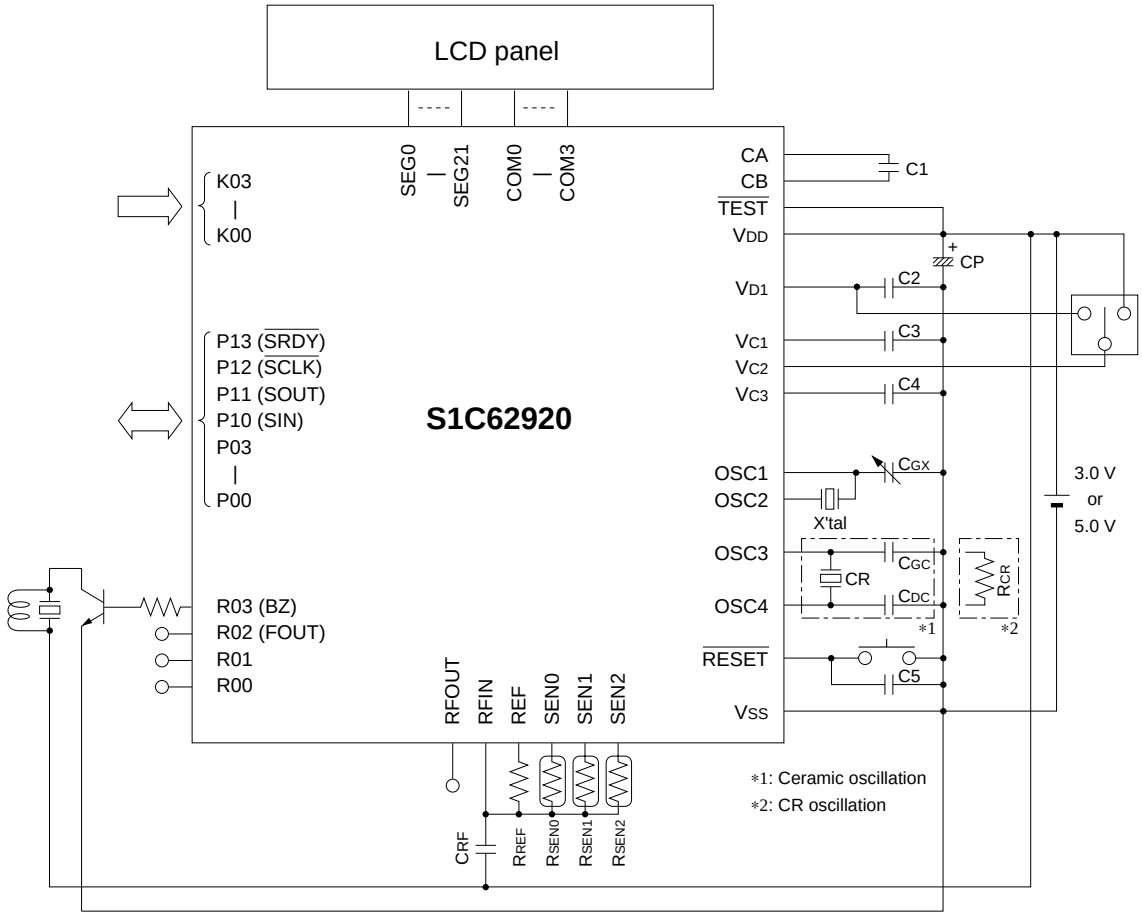
(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

Interrupt and HALT

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

CHAPTER 6 DIAGRAM OF BASIC EXTERNAL CONNECTIONS



X'tal	Crystal oscillator	32.768 kHz, C_I (Max.) = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	1 MHz (Typ.)
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
R_{CR}	CR oscillating resistor	33 kΩ (1,000 kHz, Typ.)
R_{REF}	Reference resistance for R/F conversion	50 kΩ
R_{SEN0}	Sensor 0 for R/F conversion (DC bias)	503AT-2 *3
R_{SEN1}	Sensor 1 for R/F conversion (DC bias)	503AT-2 *3
R_{SEN2}	Sensor 2 for R/F conversion (DC bias)	503AT-2 *3
C_{RF}	Capacitor for R/F conversion	2,200 pF
C1–C5	Capacitor	0.1 µF
CP	Power capacitor	3.3 µF

*3: Made by Ishizuka Electronics Corporation

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{SS} = 0 V)

Item	Symbol	Rated value	Unit
Power voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-40 to 85	°C
Strage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible disspation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).
*2 In case of plastic package (QFP6-64pin, QFP13-64pin).

7.2 Recommended Operating Conditions

(Ta = -40 to 85°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power voltage	V_{DD}	V_{SS} = 0 V	When V_{C2} is connected to V_{D1}	2.2	3.0	5.5	V
			When V_{C2} is connected to V_{DD}	2.2	3.0	3.6	V
Oscillation frequency	f_{OSC1}			–	32.768	–	kHz
	f_{OSC3}	Duty 50±10%		300	1,000	1,300	kHz

7.3 DC Characteristics

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, V_{D1}/V_{C1}/V_{C3} are internal voltage, V_{C2} is external voltage, C1–C5 = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input threshold voltage	V_{IKH}	L → H	K00–K03	1.80	2.25	2.70	V
	V_{IKL}	H → L	K00–K03	0.35	0.60	0.85	V
High level input voltage (1)	V_{IH1}		P00–P03, P10–P13	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		P00–P03, P10–P13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current (1)	I_{IH1}	V_{IH1} = 3.0 V	K00–K03	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2} = 3.0 V	P00–P03, P10–P13 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1} = V_{SS} Without pull up resistor	K00–K03	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2} = V_{SS} Without pull up resistor	P00–P03, P10–P13 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (3)	I_{IL3}	V_{IL3} = V_{SS} With pull up resistor	K00–K03	-15	-8	-5	µA
Low level input current (4)	I_{IL4}	V_{IL4} = V_{SS} With pull up resistor	P00–P03, P10–P13 $\overline{RESET}$, $\overline{TEST}$	-15	-8	-5	µA
High level output current (1)	I_{OH1}	V_{OH1} = 0.9·V_{DD}	R00–R03			-4.0	mA
High level output current (2)	I_{OH2}	V_{OH2} = 0.9·V_{DD}	P00–P03, P10–P13 RFOUT			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1} = 0.1·V_{DD}	R00–R03	6			mA
Low level output current (2)	I_{OL2}	V_{OL2} = 0.1·V_{DD}	P00–P03, P10–P13 RFOUT	6			mA
Common output current	I_{OH3}	V_{OH3} = V_{C3} - 0.05 V	COM0–COM3			-3	µA
	I_{OL3}	V_{OL3} = V_{SS} + 0.05 V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4} = V_{C3} - 0.05 V	SEG0–SEG21			-3	µA
	I_{OL4}	V_{OL4} = V_{SS} + 0.05 V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5} = 0.9·V_{DD}	SEG0–SEG21			-200	µA
	I_{OL5}	V_{OL5} = 0.1·V_{DD}		200			µA

7.4 Analog Characteristics and Consumed Current

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, f_{OSC1} = 32.768 kHz, C_G = 25 pF, C_{RF} = 2,200 pF, R_{REF} = 50 kΩ, Ta = 25°C,

V_{D1}/V_{C1}/V_{C3} are internal voltage, V_{C2} is external voltage, C1–C5 = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	V_{C2} = V_{DD}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (Without panel load)	1/2 V_{DD} × 0.9	1/2 V_{DD}	1/2 V_{DD} + 0.1	V
		V_{C2} = V_{D1}		1/2 V_{D1} × 0.9	1/2 V_{D1}	1/2 V_{D1} + 0.1	V
	V_{C2}	V_{C2} = V_{DD}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (Without panel load)		V_{DD}		V
		V_{C2} = V_{D1}		1.9	2.1	2.3	V
	V_{C3}	V_{C2} = V_{DD}	Connect 1MΩ load resistor between V_{SS} and V_{C3} (Without panel load)	3/2 V_{DD} × 0.9	3/2 V_{DD}	3/2 V_{DD} + 0.1	V
		V_{C2} = V_{D1}		3/2 V_{D1} × 0.9	3/2 V_{D1}	3/2 V_{D1} + 0.1	V
SVD voltage	V_{SVD}	2.4 V (mask option setting)		2.22	2.4	2.58	V
		2.5 V (mask option setting)		2.30	2.5	2.70	V
		2.6 V (mask option setting)		2.38	2.6	2.82	V
		2.7 V (mask option setting)		2.46	2.7	2.94	V
SVD circuit responce time	t_{SVD}					100	µS
Power current consumption	I_{OP}	During HALT (32 kHz)	Without panel load		2	6	µA
		During execution (32 kHz) *1			5	9	nA
		During execution (1 MHz) *1			270	500	µA
		During execution (32 kHz) *2			40	120	µA
		During execution (32 kHz) *3			11	30	µA

*1 The R/F converter and SVD circuit are in OFF status.
*2 The R/F converter is in ON status. The SVD circuit is in OFF status.
*3 The R/F converter is in OFF status. The SVD circuit is in ON status.

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, Crystal: Q13MC146, CI = 35 kΩ, C_G = 25 pF, C_D = built-in, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta ≤ 3 sec (V_{DD})	2.2			V
Oscillation stop voltage	Vstp	tstp ≤ 10 sec (V_{DD})	2.2			V
Built-in capacitance (drain)	C_D	Including incidental capacitance inside IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{DD} = 2.2 to 5.5 V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G = 5 to 25 pF	35			ppm
Harmonic oscillation start voltage	V_{hho}	C_G = 5 pF (V_{DD})			7	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

OSC3 CR oscillation circuit

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, R_{CR} = 33 kΩ, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	(1 MHz)	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD} = 2.2 to 5.5 V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 ceramic oscillation circuit

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, Ceramic oscillator: 1 MHz, C_{GC} = C_{DC} = 100 pF, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD} = 2.2 to 5.5 V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

7.6 CR Oscillation Characteristics

The following characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

(1) CR oscillation frequency characteristic

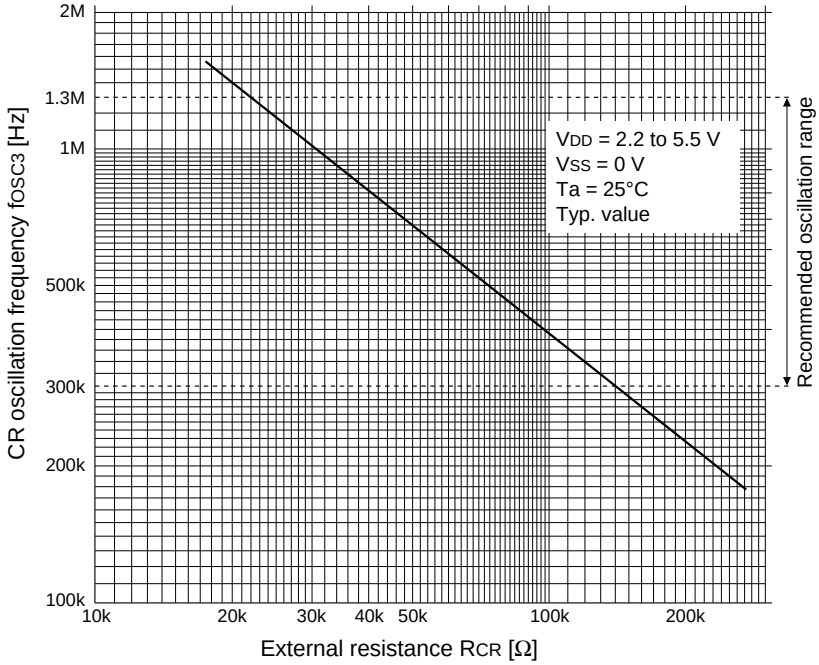


Fig. 7.6.1 CR oscillation characteristic

(2) Frequency-Current consumption characteristic

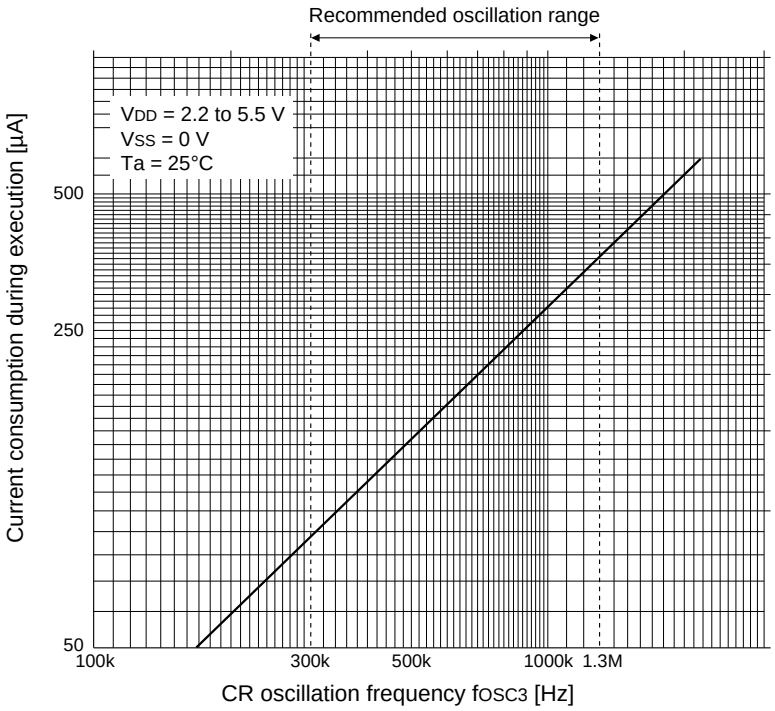


Fig. 7.6.2 Frequency-current consumption characteristic

7.7 R/F Converter Characteristics

The following characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, f_{OSC1} = 32.768 kHz, C_{RF} = 2,200 pF, R_{REF} = 10 kΩ or 50 kΩ, Ta = -40°C to 85°C
The following values do not include errors caused by changing temperature of the external attached elements (R_{REF}, C_{RF})

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
R/F conversion counter value	C_{RS1}	1 kΩ ≤ R_{SEN} < 10 kΩ	MC×0.93		MC×1.07	count
	C_{RS2}	10 kΩ ≤ R_{SEN} ≤ 2 MΩ	MC×0.97 -15		MC×1.03 +15	count

$$* \ MC = \frac{R_{REF}\,[k\Omega] + 0.15}{R_{SEN}\,[k\Omega] + 0.15} \times \text{Measurement counter value}$$

(1) Sensor resistance-Oscillation frequency ratio

Figure 7.7.1 shows the oscillation frequency ratio (ratio of oscillation frequency by the reference resistance to oscillation frequency by the sensor resistance) when the following elements are connected. (Typ.)
If the R/F conversion uses SEN0, SEN1 or SEN2, both characteristics will be the same.

Reference resistance (R_{REF}) ..... 10 kΩ
Sensor resistance (R_{SEN0}, R_{SEN1}, R_{SEN2}) ..... 10 kΩ to 20 MΩ
Oscillating capacitor (C_{RF}) ..... 2,200 pF

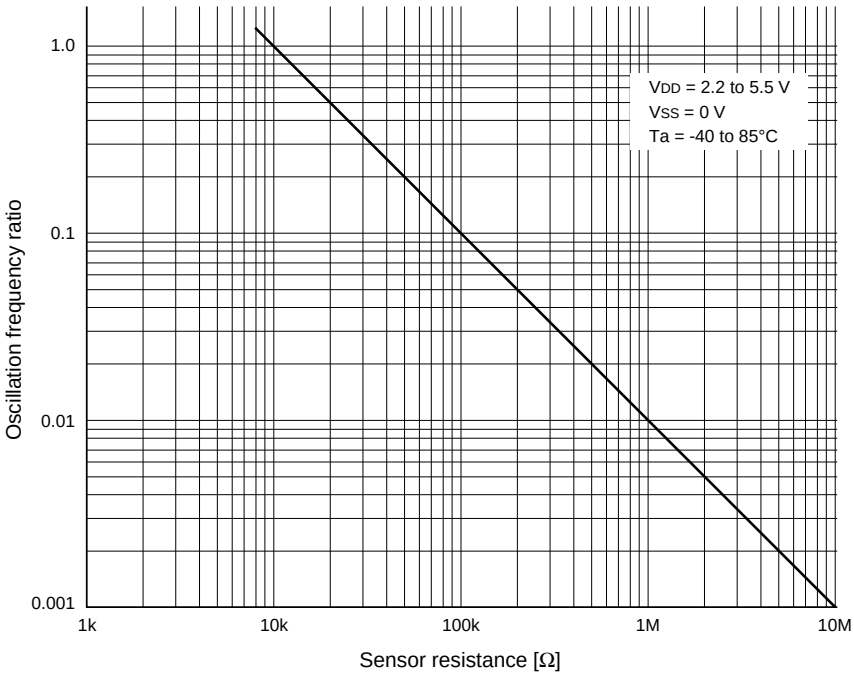


Fig. 7.7.1 Oscillation frequency ratio-resistance curve

(2) Resistance-Oscillation frequency

CR oscillation frequency of the R/F converter disperses in each sampling. Therefore, the initial setting value of the measurement counter should be decided after considering the fluctuation margin of the CR oscillation frequency by the reference resistance and sensor resistance to be used for the measurement. Figures 7.7.2 and 7.7.3 show the resistance-oscillation frequency curves.

Note: • *The following curves are characteristic when the oscillating capacitor is 2,200 pF.*
• *Typical oscillation frequency is characteristic when V_{DD} = 3.0 V and Ta = 25°C.*

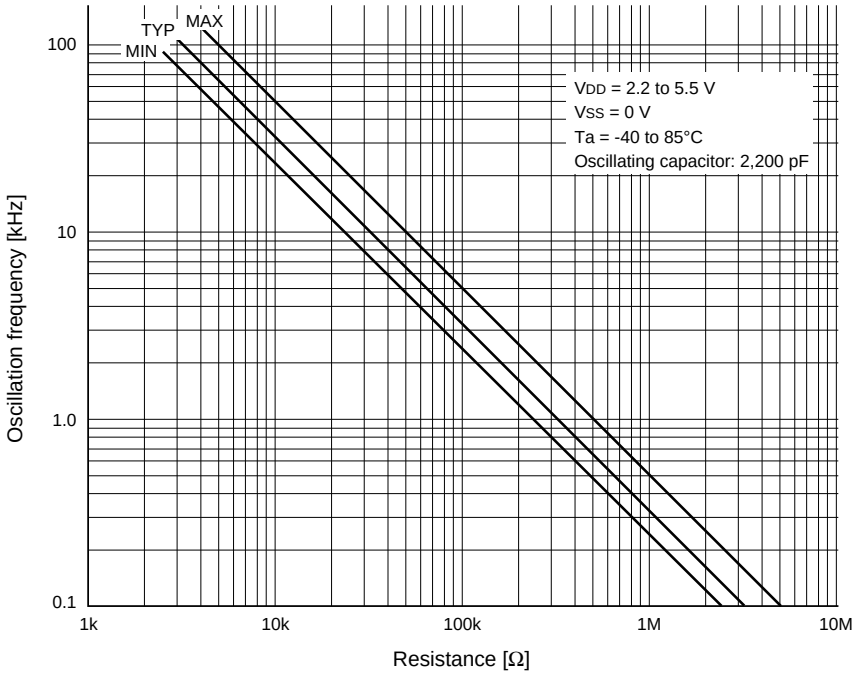


Fig. 7.7.2 Resistance-oscillation frequency curve (REF)

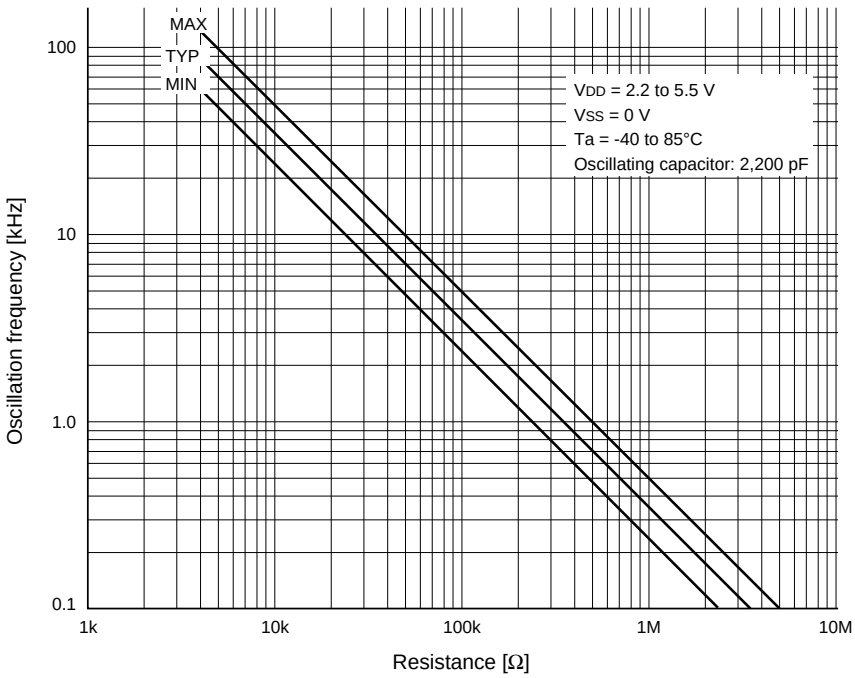


Fig. 7.7.3 Resistance-oscillation frequency curve (SEN0, SEN1, SEN2)

7.8 Serial Interface AC Characteristics

1. Clock synchronous master mode (512 Hz)

Condition: V_{DD} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

2. Clock synchronous master mode (1 MHz)

Condition: V_{DD} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

3. Clock synchronous slave mode (512 Hz)

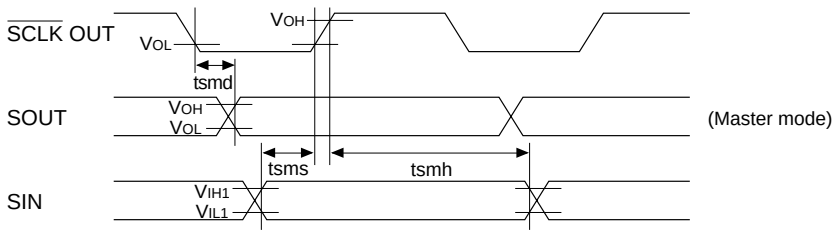
Condition: V_{DD} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

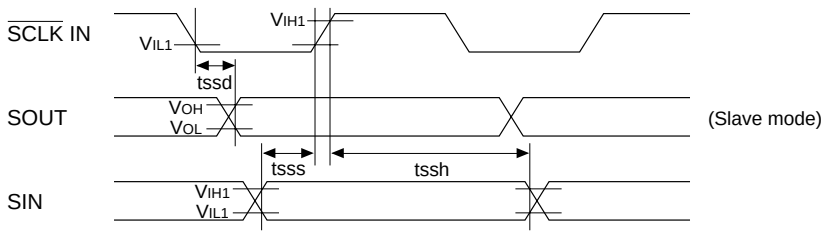
Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

4. Clock synchronous slave mode (1 MHz)

Condition: V_{DD} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS



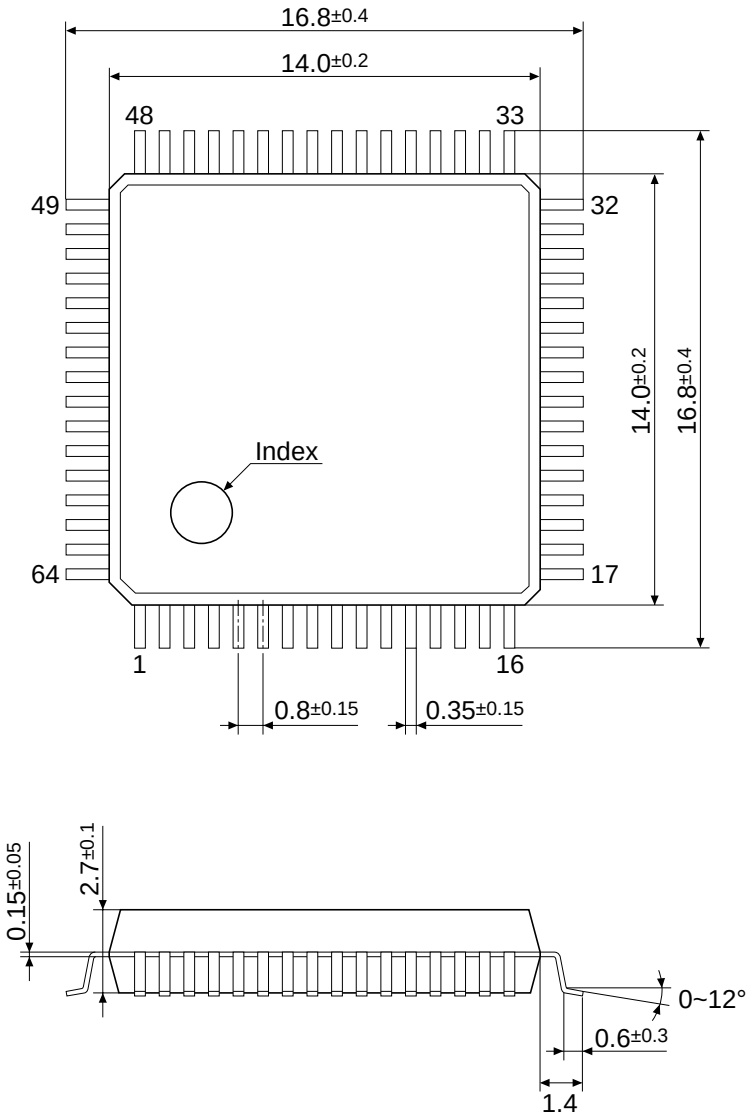


CHAPTER 8 PACKAGE

8.1 Plastic Package

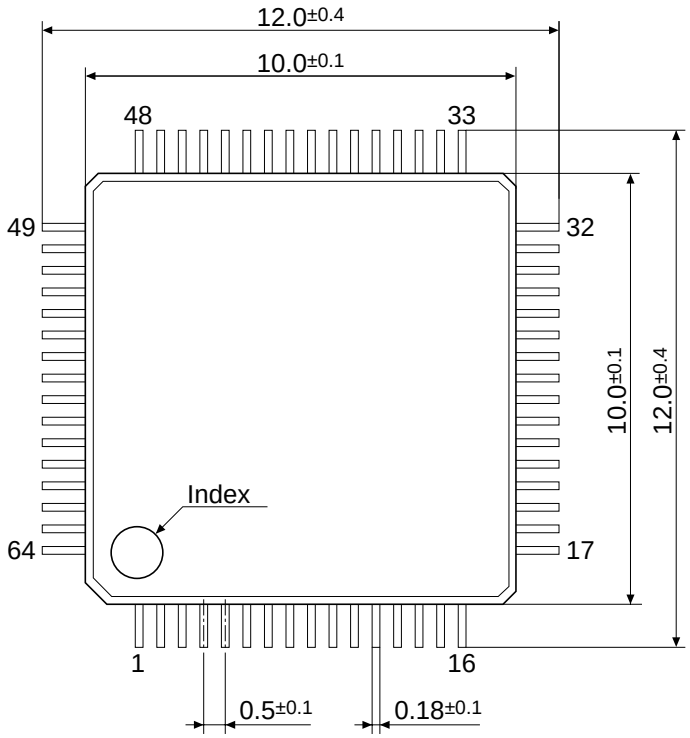
QFP6-64pin-S1

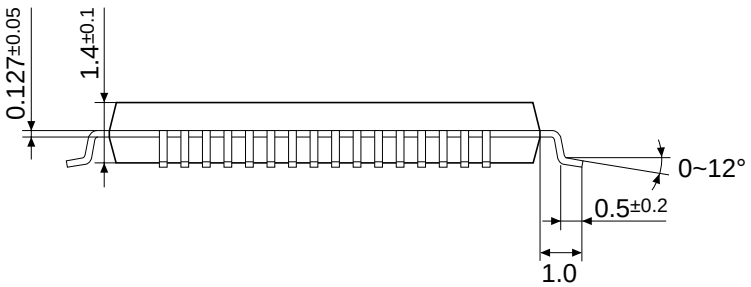
(Unit: mm)



QFP13-64pin

(Unit: mm)

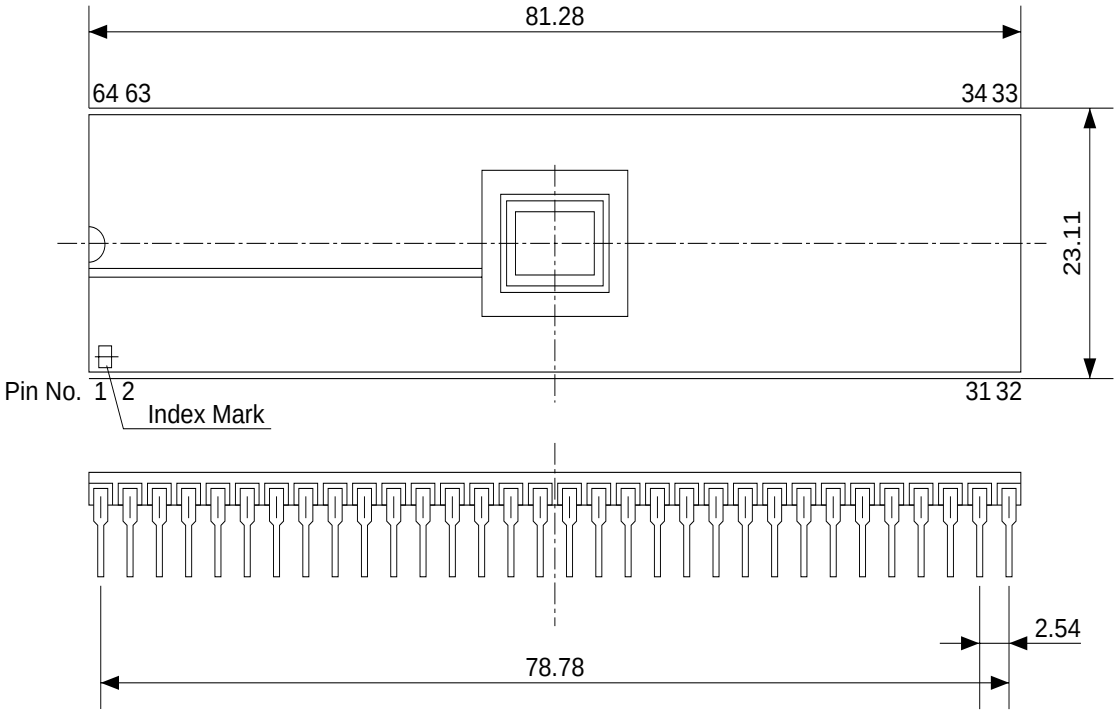




8.2 Ceramic Package for Test Samples

DIP-64pin

(Unit: mm)

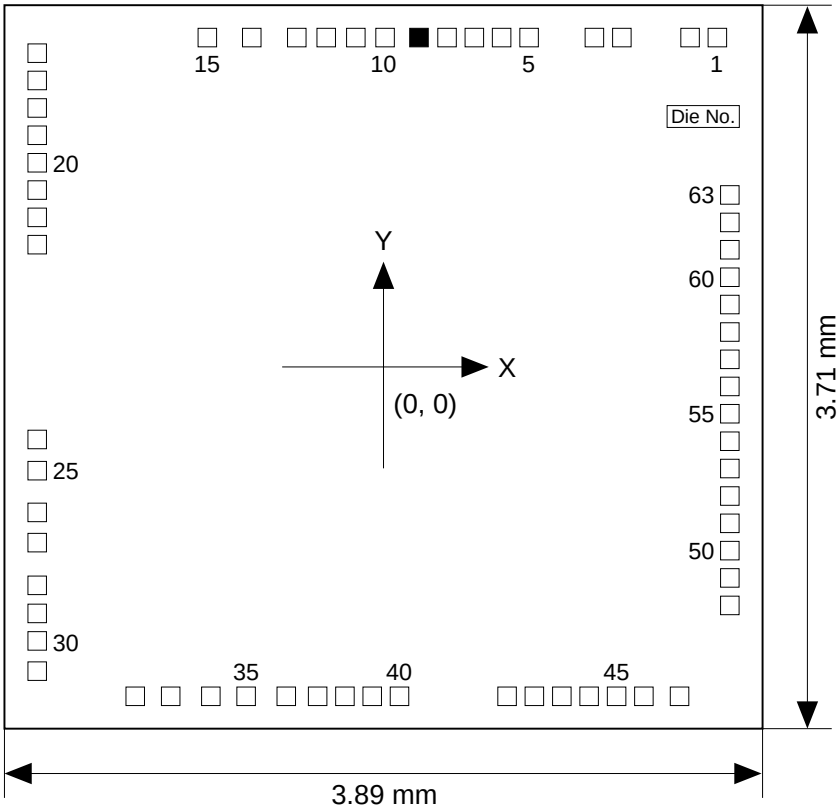


Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	17	V_{SS}	33	SEG0	49	SEG15
2	REF	18	OSC1	34	SEG1	50	SEG16
3	SEN0	19	OSC2	35	SEG2	51	SEG17
4	SEN1	20	V_{DD}	36	SEG3	52	SEG18
5	SEN2	21	OSC4	37	SEG4	53	SEG19
6	RFIN	22	OSC3	38	SEG5	54	SEG20
7	RFOUT	23	V_{D1}	39	$\overline{TEST}$	55	SEG21
8	P13	24	V_{C2}	40	SEG6	56	R03
9	P12	25	V_{C1}	41	SEG7	57	R02
10	P11	26	V_{C3}	42	SEG8	58	R01
11	P10	27	CA	43	SEG9	59	R00
12	P03	28	CB	44	SEG10	60	K03
13	P02	29	COM3	45	SEG11	61	K02
14	P01	30	COM2	46	SEG12	62	K01
15	P00	31	COM1	47	SEG13	63	K00
16	$\overline{RESET}$	32	COM0	48	SEG14	64	N.C.

N.C. = No Connection

CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 95 µm

9.2 Pad Coordinates

Pad		Coordinate		Pad		Coordinate	
No.	Name	X [μm]	Y [μm]	No.	Name	X [μm]	Y [μm]
1	R03	1,713	1,689	33	V_{C1}	-1,092	-1,689
2	R02	1,573	1,689	34	V_{C3}	-886	-1,689
3	R01	1,223	1,689	35	CA	-705	-1,689
4	R00	1,082	1,689	36	CB	-499	-1,689
5	K03	747	1,689	37	COM3	-338	-1,689
6	K02	606	1,689	38	COM2	-198	-1,689
7	K01	466	1,689	39	COM1	-58	-1,689
8	K00	326	1,689	40	COM0	82	-1,689
9	N.C.	182	1,689	41	SEG0	634	-1,689
10	REF	8	1,689	42	SEG1	774	-1,689
11	SEN0	-142	1,689	43	SEG2	915	-1,689
12	SEN1	-294	1,689	44	SEG3	1,055	-1,689
13	SEN2	-445	1,689	45	SEG4	1,196	-1,689
14	RFIN	-676	1,689	46	SEG5	1,336	-1,689
15	RFOUT	-904	1,689	47	$\overline{TEST}$	1,519	-1,689
16	P13	-1,777	1,609	48	SEG6	1,777	-1,223
17	P12	-1,777	1,469	49	SEG7	1,777	-1,082
18	P11	-1,777	1,328	50	SEG8	1,777	-942
19	P10	-1,777	1,188	51	SEG9	1,777	-802
20	P03	-1,777	1,047	52	SEG10	1,777	-662
21	P02	-1,777	907	53	SEG11	1,777	-521
22	P01	-1,777	767	54	SEG12	1,777	-381
23	P00	-1,777	627	55	SEG13	1,777	-240
24	$\overline{RESET}$	-1,777	-372	56	SEG14	1,777	-100
25	V_{SS}	-1,777	-532	57	SEG15	1,777	39
26	OSC1	-1,777	-746	58	SEG16	1,777	179
27	OSC2	-1,777	-901	59	SEG17	1,777	320
28	V_{DD}	-1,777	-1,120	60	SEG18	1,777	460
29	OSC4	-1,777	-1,264	61	SEG19	1,777	601
30	OSC3	-1,777	-1,405	62	SEG20	1,777	741
31	V_{D1}	-1,777	-1,560	63	SEG21	1,777	882
32	V_{C2}	-1,274	-1,689				

APPENDIX A. S1C62920 RAM MAP

RAM map (000H–07FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NAME MSB															
																	LSB
	1	NAME MSB															
																	LSB
	2	NAME MSB															
																	LSB
	3	NAME MSB															
																	LSB
	4	NAME MSB															
																	LSB
	5	NAME MSB															
																	LSB
	6	NAME MSB															
																	LSB
	7	NAME MSB															
																	LSB

Display memory map (160H–17FH, W only)

PROGRAM NAME:															
P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	6	NAME MSB															
		LSB															
	7	NAME MSB															
		LSB															

I/O memory map (80H–FCH)

PROGRAM NAME:

P	H \ L		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	8	NAME																
		MSB	0	0														
1			0	0														
			SVDDT	CLKCHG														
		LSB	SVDON	OSCC														
	9	NAME																
		MSB		K03	KCP03													
				K02	KCP02													
				K01	KCP01													
		LSB		K00	KCP00													
	A	NAME																
		MSB	R03															
			R02															
			R01															
		LSB	R00															
	B	NAME																
		MSB	IOC03		P03		IOC13		P13									
			IOC02		P02		IOC12		P12									
			IOC01		P01		IOC11		P11									
		LSB	IOC00		P00		IOC10		P10									
	C	NAME																
		MSB		0					0		0	TM3	TM7					
				0					0		0	TM2	TM6					
				LOFF					0		TMRUN	TM1	TM5					
		LSB		LPWR					WDRST		TMRST	TM0	TM4					
	D	NAME																
		MSB	DBGOS	0	OVTBC	MC03	MC07	MC11	MC15									
			RFDBG	0	OVMC	MC02	MC06	MC10	MC14									
			RFCLK	SENS1	RFRUN	MC01	MC05	MC09	MC13									
		LSB	0	SENS0	0	MC00	MC04	MC08	MC12									
	E	NAME																
		MSB									SCS0	SD3	SD7					
											0	SD2	SD6					
											SCTRG	SD1	SD5					
		LSB									ESIF	SD0	SD4					
	F	NAME																
		MSB	0	0		0	0				0	0		0	0			
			0	0		0	EIT2				0	0		0	IT2			
			0	0		0	EIT1				0	0		0	IT1			
		LSB	EISIF	EIRF		EIK0	EIT0				ISIF	IRF		IK0	IT0			

Unused area

APPENDIX B. S1C62920 INSTRUCTION SET

Classification	Mne-monic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	*l*	0	0	0	1	*l* 7	*l* 6	*l* 5	*l* 4	*l* 3	*l* 2	*l* 1	*l* 0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← *l* 3~*l* 0, M(X+1) ← *l* 7~*l* 4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

Classification	Mne-monic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r←i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r←q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A←M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B←M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X)←i3~i0, X←X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r←q, X←X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y)←i3~i0, Y←Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r←q, Y←Y+1
	LBPX	MX, *l*	1	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					5	M(X)←*l*3~*l*0, M(X+1)←*l*7~*l*4, X←X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F←F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F←F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D←1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D←0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ←1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ←0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP←SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP←SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP←SP-1, M(SP)←r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP←SP-1, M(SP)←XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP←SP-1, M(SP)←XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP←SP-1, M(SP)←XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP←SP-1, M(SP)←YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP←SP-1, M(SP)←YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP←SP-1, M(SP)←YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP←SP-1, M(SP)←F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r←M(SP), SP←SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP←M(SP), SP←SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH←M(SP), SP←SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL←M(SP), SP←SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP←M(SP), SP←SP+1

Classification	Mne-monic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP←SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL← M(SP), SP←SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F←M(SP), SP←SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↕	↕		7	r← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↕	↕		7	r← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↕	↕		7	r← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↕	↕		7	r← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∧ i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↕			7	r← r∧ q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↕			7	r← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↕			7	r← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↕			7	r← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0		↕	↕		7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↕	↕		7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↕			7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↕			7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↕	↕		7	d3←d2, d2←d1, d1←d0, d0 ←C, C← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↕	↕		5	d3←C, d2←d3, d1←d2, d0←d1, C← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ←M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ←M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↕	↕		7	M(X) ←M(X)+r+C, X ←X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↕	↕		7	M(Y) ←M(Y)+r+C, Y ←Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↕	↕		7	M(X) ←M(X)-r-C, X ← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↕	↕		7	M(Y) ←M(Y)-r-C, Y ← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↕			7	r←$\overline{r}$

Abbreviations used in the explanations have the following meanings.

Symbols associated with registers and memory

A A register
B B register
X XHL register (low order eight bits of index register IX)
Y YHL register (low order eight bits of index register IY)
XH XH register (high order four bits of XHL register)
XL XL register (low order four bits of XHL register)
YH YH register (high order four bits of YHL register)
YL YL register (low order four bits of YHL register)
XP XP register (high order four bits of index register IX)
YP YP register (high order four bits of index register IY)
SP Stack pointer SP
SPH High-order four bits of stack pointer SP
SPL Low-order four bits of stack pointer SP
MX, M(X) Data memory whose address is specified with index register IX
MY, M(Y) Data memory whose address is specified with index register IY
Mn, M(n) Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP) Data memory whose address is specified with stack pointer SP
r, q Two-bit register code
r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Register specified
r1	r0	q1	q0	
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP New bank pointer
NPP New page pointer
PCB Program counter bank
PCP Program counter page
PCS Program counter step
PCSH Four high order bits of PCS
PCSL Four low order bits of PCS

Symbols associated with flags

F Flag register (I, D, Z, C)
C Carry flag
Z Zero flag
D Decimal flag
I Interrupt flag
↓ Flag reset
↑ Flag set
↕ Flag set or reset

Associated with immediate data

p Five-bit immediate data or label 00H–1FH
s Eight-bit immediate data or label 00H–0FFH
l Eight-bit immediate data 00H–0FFH
i Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+ Add
- Subtract
∧ Logical AND
∨ Logical OR
∀ Exclusive-OR
★ Add-subtract instruction for decimal operation when the D flag is set

APPENDIX C. PSEUDO-INSTRUCTION TABLE OF THE CROSS ASSEMBLER

Item No.	Pseudo-instruction	Meaning	Example of use
1	EQU (Equation)	To allocate data to label	`ABC EQU 9` `BCD EQU ABC+1`
2	ORG (Origin)	To define location counter	`ORG 100H` `ORG 256`
3	SET (Set)	To allocate data to label (data can be changed)	`ABC SET 0001H` `ABC SET 0002H`
4	DW (Define Word)	To define ROM data	`ABC DW 'AB'` `BCD DW 0FFBH`
5	PAGE (Page)	To define boundary of page	`PAGE 1H` `PAGE 4`
6	SECTION (Section)	To define boundary of section	`SECTION`
7	END (End)	To terminate assembly	`END`
8	MACRO (Macro)	To define macro	`CHECK MACRO DATA`

9	LOCAL
	(Local)
		To make local specification of label
		during macro definition
			`LOCAL LOOP`
			`LOOP CP MX,DATA`
			`JP NZ,LOOP`

10	ENDM (End Macro)	To end macro definition	`ENDM` `CHECK 1`

APPENDIX D. COMMAND TABLE OF ICE

Item No.	Function	Command Format	Outline of Operation
1	Assemble	#A,a ↵	Assemble command mnemonic code and store at address "a"
2	Disassemble	#L,a1,a2 ↵	Contents of addresses a1 to a2 are disassembled and displayed
3	Dump	#DP,a1,a2 ↵	Contents of program area a1 to a2 are displayed
		#DD,a1,a2 ↵	Content of data area a1 to a2 are displayed
4	Fill	#FP,a1,a2,d ↵	Data d is set in addresses a1 to a2 (program area)
		#FD,a1,a2,d ↵	Data d is set in addresses a1 to a2 (data area)
5	Set Run Mode	#G,a ↵	Program is executed from the "a" address
		#TIM ↵	Execution time and step counter selection
		#OTF ↵	On-the-fly display selection
6	Trace	#T,a,n ↵	Executes program while displaying results of step instruction from "a" address
		#U,a,n ↵	Displays only the final step of #T,a,n
7	Break	#BA,a ↵ #BAR,a ↵	Sets Break at program address "a" Breakpoint is canceled
		#BD ↵ #BDR ↵	Break condition is set for data RAM Breakpoint is canceled
		#BR ↵ #BRR ↵	Break condition is set for Evaluation Board CPU internal registers Breakpoint is canceled
		#BM ↵ #BMR ↵	Combined break conditions set for program data RAM address and registers Cancel combined break conditions for program data ROM address and registers
		#BRES ↵	All break conditions canceled
		#BC ↵	Break condition displayed
		#BE ↵	Enter break enable mode
		#BSYN ↵	Enter break disable mode
		#BT ↵	Set break stop/trace modes
		#BRKSEL,REM ↵	Set BA condition clear/remain modes
8	Move	#MP,a1,a2,a3 ↵	Contents of program area addresses a1 to a2 are moved to addresses a3 and after
		#MD,a1,a2,a3 ↵	Contents of data area addresses a1 to a2 are moved to addresses a3 and after
9	Data Set	#SP,a ↵	Data from program area address "a" are written to memory
		#SD,a ↵	Data from data area address "a" are written to memory
10	Change CPU Internal Registers	#DR ↵	Display Evaluation Board CPU internal registers
		#SR ↵	Set Evaluation Board CPU internal registers
		#I ↵	Reset Evaluation Board CPU
		#DXY ↵	Display X, Y, MX and MY
		#SXY ↵	Set data for X and Y display and MX, MY

Item No.	Function	Command Format	Outline of Operation
11	History	#H,p1,p2 ↵	Display history data for pointer 1 and pointer 2
		#HB ↵	Display upstream history data
		#HG ↵	Display 21 line history data
		#HP ↵	Display history pointer
		#HPS,a ↵	Set history pointer
		#HC,S/C/E ↵	Sets up the history information acquisition before (S), before/after (C) and after (E)
		#HA,a1,a2 ↵	Sets up the history information acquisition from program area a1 to a2
		#HAR,a1,a2 ↵	Sets up the prohibition of the history information acquisition from program area a1 to a2
		#HAD ↵	Indicates history acquisition program area
		#HS,a ↵	Retrieves and indicates the history information which executed a program address "a"
		#HSW,a ↵ #HSR,a ↵	Retrieves and indicates the history information which wrote or read the data area address "a"
12	File	#RF,file ↵	Move program file to memory
		#RFD,file ↵	Move data file to memory
		#VF,file ↵	Compare program file and contents of memory
		#VFD,file ↵	Compare data file and contents of memory
		#WF,file ↵	Save contents of memory to program file
		#WFD,file ↵	Save contents of memory to data file
		#CL,file ↵	Load ICE set condition from file
		#CS,file ↵	Save ICE set condition to file
		#OPTLD,1,file ↵ #OPTLD,2,file ↵	Load function option data from file Load segment option data from file
13	Coverage	#CVD ↵	Indicates coverage information
		#CVR ↵	Clears coverage information
14	ROM Access	#RP ↵	Move contents of ROM to program memory
		#VP ↵	Compare contents of ROM with contents of program memory
		#ROM ↵	Set ROM type
15	Terminate ICE	#Q ↵	Terminate ICE and return to operating system control
16	Command Display	#HELP ↵	Display ICE instruction
17	Self Diagnosis	#CHK ↵	Report results of ICE self diagnostic test

↵ means press the RETURN key.

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First issue December, 1994
Printed March, 2001 in Japan ⓂA