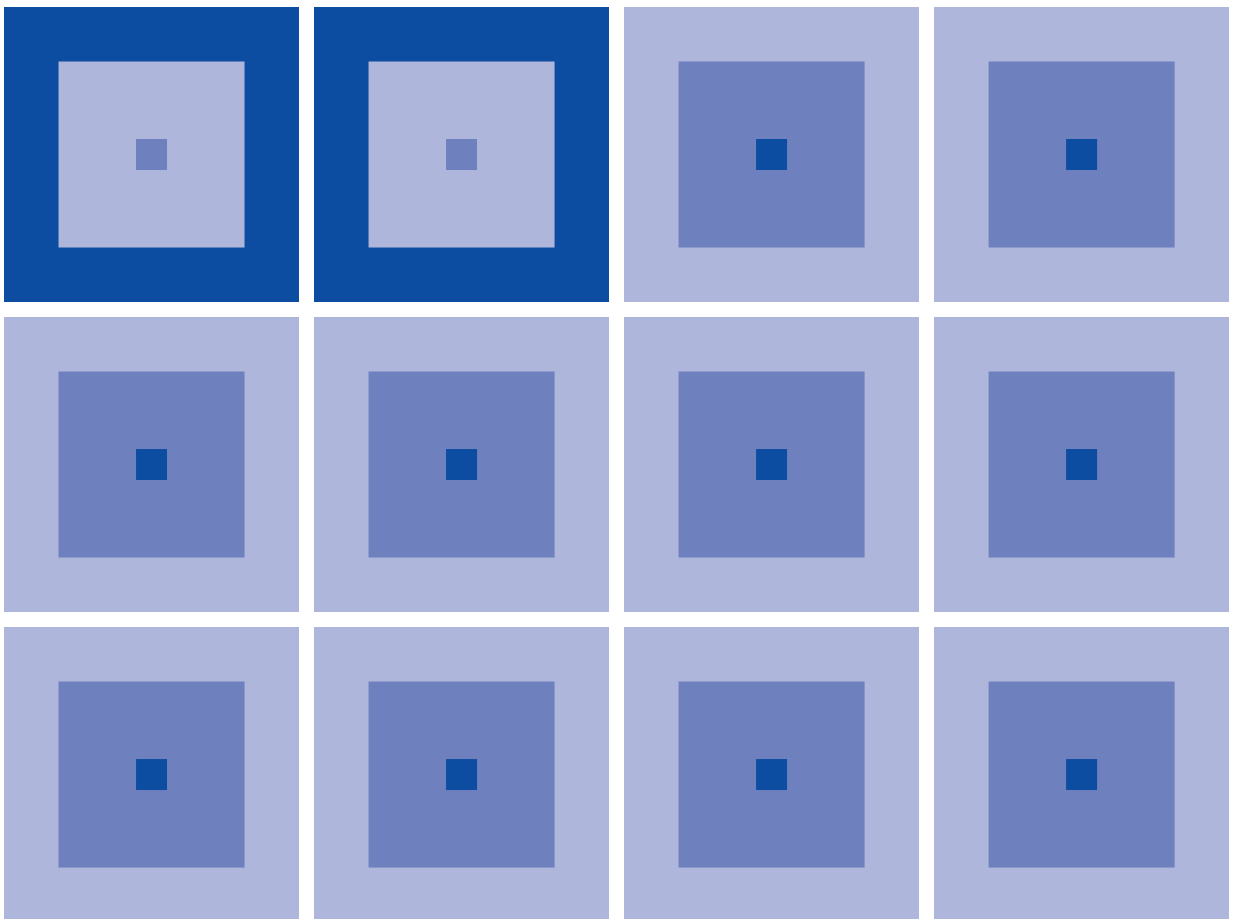


CMOS 4-BIT SINGLE CHIP MICROCOMPUTER  
**S5U1C60N02D** Manual  
(Development Software Tool for S1C60N02)



## ***NOTICE***

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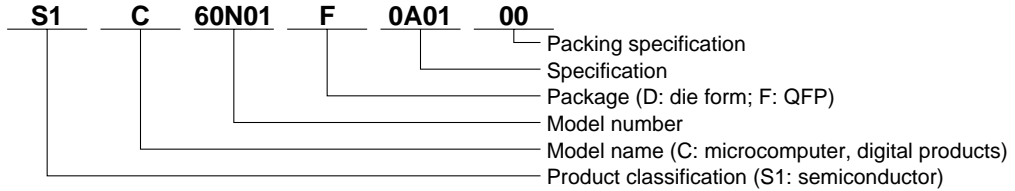
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## The information of the product number change

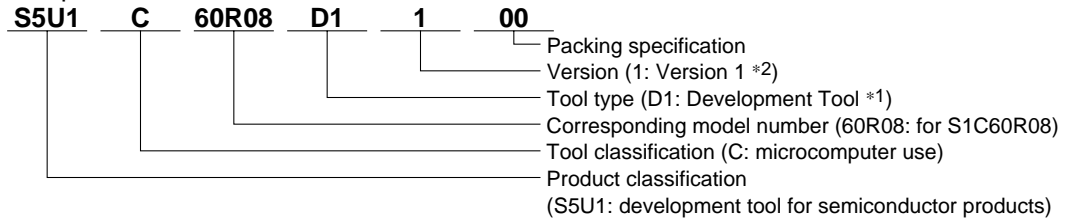
Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

## Configuration of product number

Devices



Development tools



\*1: For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)

\*2: Actual versions are not written in the manuals.

## Comparison table between new and previous number

S1C60 Family processors

Previous No.	New No.
E0C6001	S1C60N01
E0C6002	S1C60N02
E0C6003	S1C60N03
E0C6004	S1C60N04
E0C6005	S1C60N05
E0C6006	S1C60N06
E0C6007	S1C60N07
E0C6008	S1C60N08
E0C6009	S1C60N09
E0C6011	S1C60N11
E0C6013	S1C60N13
E0C6014	S1C60140
E0C60R08	S1C60R08

S1C62 Family processors

Previous No.	New No.
E0C621A	S1C621A0
E0C6215	S1C62150
E0C621C	S1C621C0
E0C6S27	S1C6S2N7
E0C6S37	S1C6S3N7
E0C623A	S1C6N3A0
E0C623E	S1C6N3E0
E0C6S32	S1C6S3N2
E0C6233	S1C62N33
E0C6235	S1C62N35
E0C623B	S1C6N3B0
E0C6244	S1C62440
E0C624A	S1C624A0
E0C6S46	S1C6S460

Previous No.	New No.
E0C6247	S1C62470
E0C6248	S1C62480
E0C6S48	S1C6S480
E0C624C	S1C624C0
E0C6251	S1C62N51
E0C6256	S1C62560
E0C6292	S1C62920
E0C6262	S1C62N62
E0C6266	S1C62660
E0C6274	S1C62740
E0C6281	S1C62N81
E0C6282	S1C62N82
E0C62M2	S1C62M20
E0C62T3	S1C62T30

## Comparison table between new and previous number of development tools

Development tools for the S1C60/62 Family

Previous No.	New No.
ASM62	S5U1C62000A
DEV6001	S5U1C60N01D
DEV6002	S5U1C60N02D
DEV6003	S5U1C60N03D
DEV6004	S5U1C60N04D
DEV6005	S5U1C60N05D
DEV6006	S5U1C60N06D
DEV6007	S5U1C60N07D
DEV6008	S5U1C60N08D
DEV6009	S5U1C60N09D
DEV6011	S5U1C60N11D
DEV60R08	S5U1C60R08D
DEV621A	S5U1C621A0D
DEV621C	S5U1C621C0D
DEV623B	S5U1C623B0D
DEV6244	S5U1C62440D
DEV624A	S5U1C624A0D
DEV624C	S5U1C624C0D
DEV6248	S5U1C62480D
DEV6247	S5U1C62470D

Previous No.	New No.
DEV6262	S5U1C62620D
DEV6266	S5U1C62660D
DEV6274	S5U1C62740D
DEV6292	S5U1C62920D
DEV62M2	S5U1C62M20D
DEV6233	S5U1C62N33D
DEV6235	S5U1C62N35D
DEV6251	S5U1C62N51D
DEV6256	S5U1C62560D
DEV6281	S5U1C62N81D
DEV6282	S5U1C62N82D
DEV6S27	S5U1C6S2N7D
DEV6S32	S5U1C6S3N2D
DEV6S37	S5U1C6S3N7D
EVA6008	S5U1C60N08E
EVA6011	S5U1C60N11E
EVA621AR	S5U1C621A0E2
EVA621C	S5U1C621C0E
EVA6237	S5U1C62N37E
EVA623A	S5U1C623A0E

Previous No.	New No.
EVA623B	S5U1C623B0E
EVA623E	S5U1C623E0E
EVA6247	S5U1C62470E
EVA6248	S5U1C62480E
EVA6251R	S5U1C62N51E1
EVA6256	S5U1C62N56E
EVA6262	S5U1C62620E
EVA6266	S5U1C62660E
EVA6274	S5U1C62740E
EVA6281	S5U1C62N81E
EVA6282	S5U1C62N82E
EVA62M1	S5U1C62M10E
EVA62T3	S5U1C62T30E
EVA6S27	S5U1C6S2N7E
EVA6S32R	S5U1C6S3N2E2
ICE62R	S5U1C62000H
KIT6003	S5U1C60N03K
KIT6004	S5U1C60N04K
KIT6007	S5U1C60N07K



## PREFACE

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This manual mainly explains the outline of the development support tool for the 4-bit Single Chip Micro-computer S1C60N02.

Refer to the "S1C62 Family Development Tool Reference Manual" for the details (common to all models) of each development support tool. Manuals for hardware development tools are separate, so you should also refer to the below manuals.

- Development tools*   ☞ S1C62 Family Development Tool Reference Manual  
                                   S5U1C62N51E1 Manual (Evaluation Board for S1C60N01/60N02/60N05/62N51/6S3N7)  
                                   S5U1C62000H Manual (S1C60/62 Family In-Circuit Emulator)
- Device (S1C60N02)*   ☞ S1C60N02 Technical Manual
- Instructions*           ☞ S1C6200/6200A Core CPU Manual

\* In this manual, "ICE" and "evaluation board" indicate S5U1C62000H and S5U1C62N51E1, respectively.

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# 1 COMPOSITION OF DEVELOPMENT SUPPORT TOOL

Here we will explain the composition of the software for the development support tools, developmental environment and how to generate the execution disk.

## 1.1 Configuration of S5U1C60N02D

The below software are included in the product of the S1C60N02 development support tool S5U1C60N02D.

1. Cross Assembler ASM6002 ..... Cross assembler for program preparation
2. Function Option Generator FOG6002 ..... Function option data preparation program
3. Segment Option Generator SOG6002 ..... Segment option data preparation program
4. ICE Control Software ICS6002 ..... ICE control program
5. Mask Data Checker MDC6002 ..... Mask data preparation program

## 1.2 Developmental Environment

The software product of the development support tool S5U1C60N02D operates on the following host systems:

- IBM PC/AT (at least PC-DOS Ver. 2.0)

When developing the S1C60N02, the above-mentioned host computer, editor, P-ROM writer, printer, etc. must be prepared by the user in addition to the development tool which is normally supported by Seiko Epson.

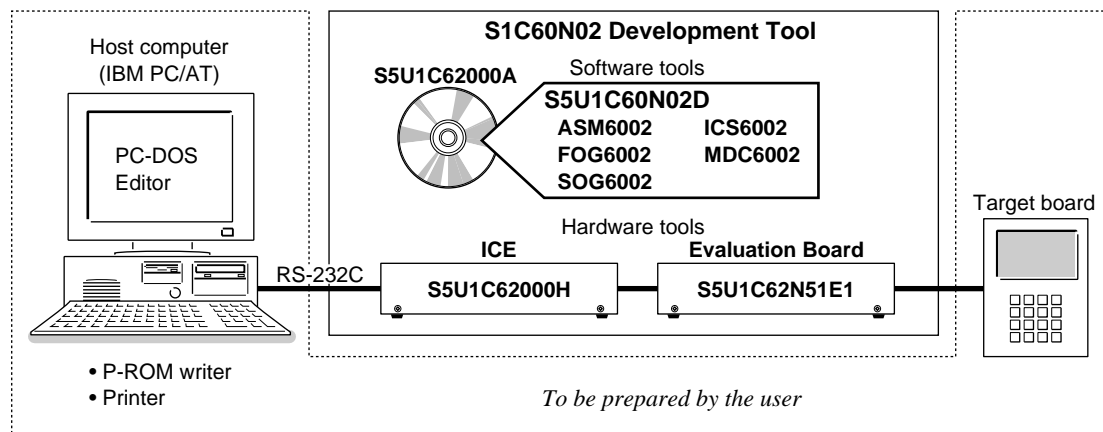


Fig. 1.2.1 System configuration

**Note** The S5U1C60N02D system requires a host computer with a RAM capacity of about 140K bytes. Since the ICE (S5U1C62000H) is connected to the host computer with a RS-232C serial interface, adapter board for asynchronous communication will be required depending on the host computer used.

### 1.3 Development Flow

Figure 1.3.1 shows the development flow through the S5U1C60N02D.

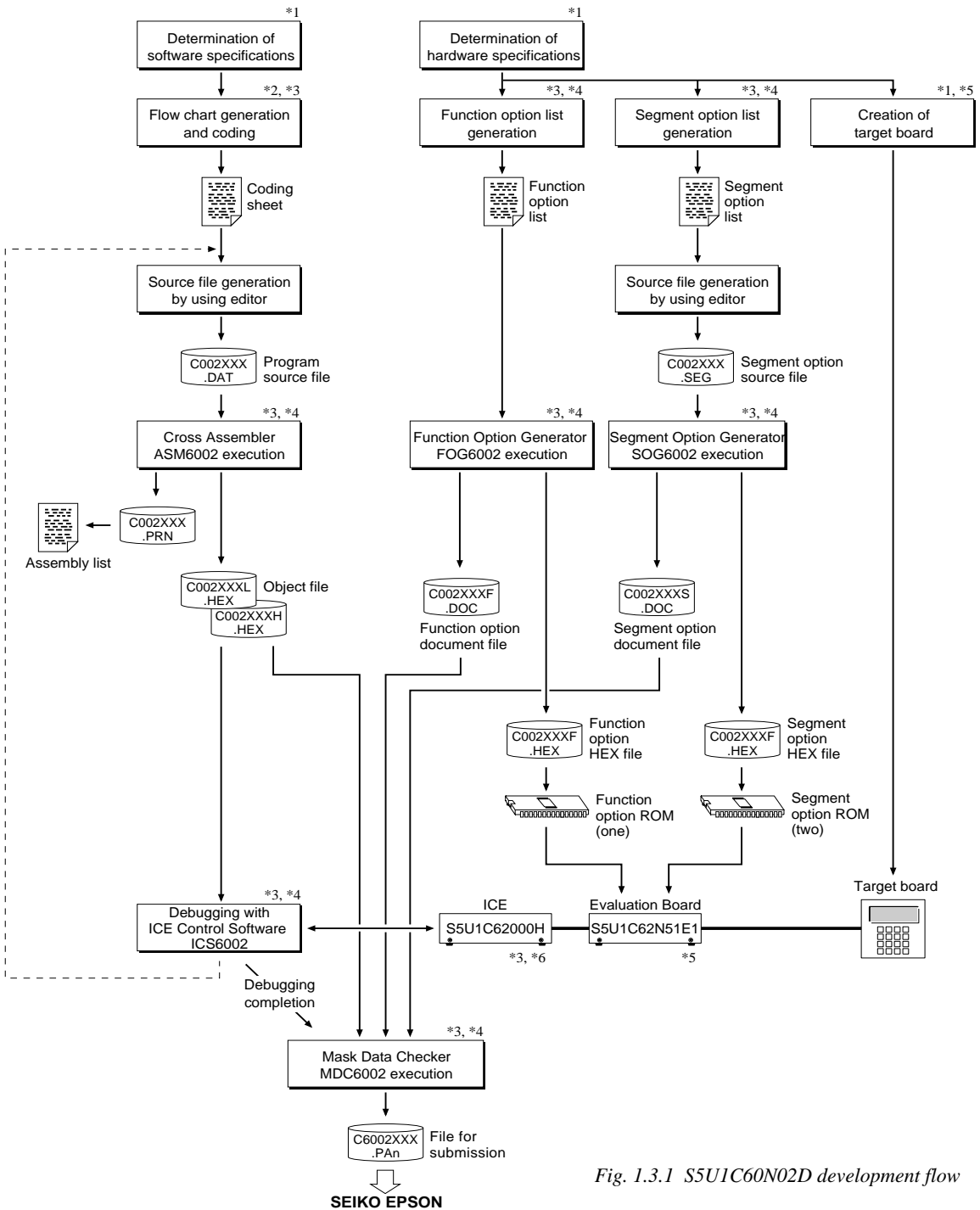


Fig. 1.3.1 S5U1C60N02D development flow

#### Concerning file names

All the input-output file name for the each development support tool commonly use "C002XXX". In principle each file should be produced in this manner. Seiko Epson will designate the "XXX" for each customer.

#### Reference Manual

- \*1 S1C60N02 Technical Manual
- \*2 S1C6200/6200A Core CPU Manual
- \*3 S1C62 Family Development Tool Reference Manual
- \*4 S5U1C60N02D Manual (this manual)
- \*5 S5U1C62N51E1 Manual
- \*6 S5U1C62000H Manual

## ***1.4 Installation***

---

The S5U1C60N02D tools are included on the CD-ROM of the S5U1C62000A (S1C60/62 Family Assembler Package), and they can be installed in your hard disk using the installer (Setup.exe) on the CD-ROM. Refer to the "S5U1C62000A Manual" for how to install the S5U1C60N02D tools.

# 2 CROSS ASSEMBLER ASM6002

## 2.1 ASM6002 Outline

The ASM6002 cross assembler is an assembler program for generating the machine code used by the S1C60N02 4-bit, single-chip microcomputers. The Cross Assembler ASM6002 will assemble the program source files which have been input by the user's editor and will generate an object file in Intel-Hex format and assembly list file. In this assembler, program modularization has been made possible through macro definition functions and programming independent of the ROM page structure has been made possible through the auto page set function. In addition, consideration has also been given to precise error checks for program capacity (ROM capacity) overflows, undefined codes and the like, and for debugging of such things as label tables for assembly list files and cross reference table supplements.

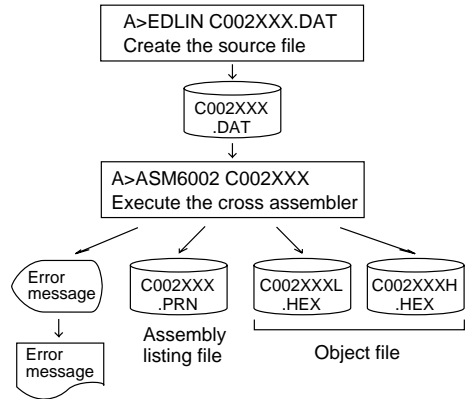


Fig. 2.1.1 ASM6002 execution flow

The format of the source file and its operating method are same as for the S1C62 Family. Refer to the "S1C62 Family Development Tool Reference Manual" for details.

## 2.2 S1C60N02 Restrictions

Note the following when generating a program by the S1C60N02:

### ROM area

The capacity of the S1C60N02 ROM is 1K steps (0000H to 03FFH). Therefore, the specification range of the memory setting pseudo-instructions and PSET instruction is restricted.

### Memory configuration:

Bank: Only bank 0, Page: 4 pages (0 to 3H), each 256 steps

### Significant specification range:

ORG pseudo-instruction: 0000H to 03FFH  
 PAGE pseudo-instruction: 00H to 03H  
 BANK pseudo-instruction: Only 0H  
 PSET instruction: 00H to 03H

### RAM area

The capacity of the S1C60N02 RAM is 129 words (000H to 04FH, 090H to 0AFH, 0E0H, 0E3H to 0E8H, 0EBH to 0EDH, 0EFH to 0F1H, and 0F3H to 0FEH, 4 bits/word). Memory access is invalid when the unused area of the index register is specified.

**Example:** LD X, 0F2H F2H is loaded into the IX register, but an unused area has been specified so that the memory accessible with the IX register (MX) is invalid.  
 LD Y, 05DH 5DH is loaded into the IY register, but an unused area has been specified so that the memory accessible with the IY register (MY) is invalid.

### Undefined codes

The following instructions have not been defined in the S1C60N02 instruction sets.

SLP			
PUSH	XP	PUSH	YP
POP	XP	POP	YP
LD	XP,r	LD	YP,r
LD	r,XP	LD	r,YP

## 2.3 ASM6002 Quick Reference

### ■ Starting command and input/output files

**Execution file:** ASM6002.EXE

*\_* indicates a blank.

indicates the Return key.

A parameter enclosed by [ ] can be omitted.

**Starting command:** **ASM6002\_ [drive-name:] source-file-name [.shp]\_ [-N]**

**Option:**

- .shp Specifies the file I/O drives.
- s Specifies the drive from which the source file is to be input. (A–P, @)
- h Specifies the drive to which the object file is to be output. (A–P, @, Z)
- p Specifies the drive to which the assembly listing file is to be output. (A–P, @, Z)
- @: Current drive, Z: File is not generated
- N The code (FFH) in the undefined area of program memory is not created.

**Input file:** C002XXX.DAT (Source file)

**Output file:**

- C002XXXL.HEX (Object file, low-order)
- C002XXXH.HEX (Object file, high-order)
- C002XXX.PRN (Assembly listing file)

### ■ Display example

```

*** E0C6002 CROSS ASSEMBLER. --- Ver 2.00 ***
EEEEEEEEEE PPPPPPPP SSSSSSS 0000000 NNN NNN
EEEEEEEEEE PPPPPPPP SSS SSSS 000 000 NNNN NNN
EEE PPP PPP SSS SSS 000 000 NNNNN NNN
EEE PPP PPP SSS 000 000 NNNNNN NNN
EEEEEEEEEE PPPPPPPP SSSSSS 000 000 NNN NNN NNN
EEEEEEEEEE PPPPPPPP SSSS 000 000 NNN NNNNNN
EEE PPP PPP SSS 000 000 NNN NNNNN
EEE PPP SSS SSS 000 000 NNN NNNN
EEEEEEEEEE PPP SSS SSS 000 000 NNN NNN
EEEEEEEEEE PPP SSSSSS 0000000 NNN NNN
(C) COPYRIGHT 1991 SEIKO EPSON CORP.
SOURCE FILE NAME IS " C002XXX.DAT "
THIS SOFTWARE MAKES NEXT FILES.
C002XXXH.HEX ... HIGH BYTE OBJECT FILE.
C002XXXL.HEX ... LOW BYTE OBJECT FILE.
C002XXX.PRN ... ASSEMBLY LIST FILE.
DO YOU NEED AUTO PAGE SET? (Y/N) Y ... (1)
DO YOU NEED CROSS REFERENCE TABLE? (Y/N) Y ... (2)

```

When ASM6002 is started, the start-up message is displayed.

At (1), select whether or not the auto-page-set function will be used.

Use ..... Y

Not use ..... N

If the assembly listing file output is specified, message (2) is displayed. At this stage, cross-reference table generation may be selected.

Generating ..... Y

Not generating ..... N

When the above operation is completed, ASM6002 assembles the source file.

To suspend execution, press the "CTRL" and "C" keys together at stage (1) or (2).

### ■ Operators

Arithmetic operators		Logical operators	
+a	Monadic positive	a_AND_b	Logical product
-a	Monadic negative	a_OR_b	Logical sum
a+b	Addition	a_XOR_b	Exclusive logical sum
a-b	Subtraction	NOT_a	Logical negation
a*b	Multiplication	Relational operators	
a/b	Division	a_EQ_b	True when a is equal to b
a_MOD_b	Remainder of a/b	a_NE_b	True when a is not equal to b
a_SHL_b	Shifts a b bits to the left	a_LT_b	True when a is less than b
a_SHR_b	Shifts a b bits to the right	a_LE_b	True when a is less than or equal to b
HIGH_a	Separates the high-order eight bits from a	a_GT_b	True when a is greater than b
LOW_a	Separates the low-order eight bits from a	a_GE_b	True when a is greater than or equal to b

## ■ Pseudo-instructions

Pseudo-instruction	Meaning	Example of use
EQU (Equation)	To allocate data to label	ABC EQU 9 BCD EQU ABC+1
SET (Set)	To allocate data to label (data can be changed)	ABC SET 0001H ABC SET 0002H
DW (Define Word)	To define ROM data	ABC DW 'AB' BCD DW 0FFBH
ORG (Origin)	To define location counter	ORG 100H ORG 256
PAGE (Page)	To define boundary of page	PAGE 1H PAGE 3
SECTION (Section)	To define boundary of section	SECTION
END (End)	To terminate assembly	END
MACRO (Macro)	To define macro	CHECK MACRO DATA LOCAL LOOP
LOCAL (Local)	To make local specification of label during macro definition	LOOP CP MX , DATA JP NZ , LOOP
ENDM (End Macro)	To end macro definition	ENDM  CHECK 1


## ■ Error messages

Error message	Explanation
S (Syntax Error)	An unrecoverable syntax error was encountered.
U (Undefined Error)	The label or symbol of the operand has not been defined.
M (Missing Label)	The label field has been omitted.
O (Operand Error)	A syntax error was encountered in the operand, or the operand could not be evaluated.
P (Phase Error)	The same label or symbol was defined more than once.
R (Range Error)	<ul style="list-style-type: none"> <li>The location counter value exceeded the upper limit of the program memory, or a location exceeding the upper limit was specified.</li> <li>A value greater than that which the number of significant digits of the operand will accommodate was specified.</li> </ul>
! (Warning)	<ul style="list-style-type: none"> <li>Memory areas overlapped because of a "PAGE" or "ORG" pseudo-instruction or both.</li> <li>A statement exceeded a page boundary although its location was not specified.</li> </ul>
FILE NAME ERROR	The source file name was longer than 8 characters.
FILE NOT PRESENT	The specified source file was not found.
DIRECTORY FULL	No space was left in the directory of the specified disk.
FATAL DISK WRITE ERROR	The file could not be written to the disk.
LABEL TABLE OVERFLOW	The number of defined labels and symbols exceeded the label table capacity (4000).
CROSS REFERENCE TABLE OVERFLOW	The label/symbol reference count exceeded the cross-reference table capacity (only when the cross-reference table is generated).

# 3 FUNCTION OPTION GENERATOR FOG6002

## 3.1 FOG6002 Outline

With the 4-bit single-chip S1C60N02 microcomputers, the customer may select 10 hardware options. By modifying the mask patterns of the S1C60N02 according to the selected options, the system can be customized to meet the specifications of the target system. The Function Option Generator FOG6002 is a software tool for generating data files used to generate mask patterns. It enables the customer to interactively select and specify pertinent items for each hardware option. From the data file created with FOG6002, the S1C60N02 mask pattern is automatically generated by a general purpose computer. The HEX file for the evaluation board (S5U1C62N51E1) hardware option ROM is simultaneously generated with the data file.

 The operating method is same as for the S1C62 Family. Refer to the "S1C62 Family Development Tool Reference Manual" for details.

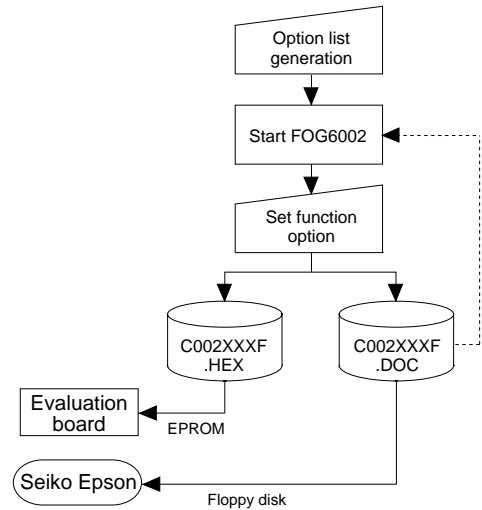


Fig. 3.1.1 FOG6002 execution flow

## 3.2 S1C60N02 Option List

Multiple specifications are available in each option item as indicated in the Option List. Using "3.3 Option Specifications and Selection Message" as reference, select the specifications that meet the target system. Be sure to record the specifications for unused ports too, according to the instructions provided.

### 1. DEVICE TYPE AND LCD VOLTAGE

- |                                      |                             |           |
|--------------------------------------|-----------------------------|-----------|
| <input type="checkbox"/> 1. E0C6002  | (Normal Type <S1C60N02>)    | LCD 3 V   |
| <input type="checkbox"/> 2. E0C6002  | (Normal Type <S1C60N02>)    | LCD 4.5 V |
| <input type="checkbox"/> 3. E0C60L02 | (Low Power Type <S1C60L02>) | LCD 3 V   |
| <input type="checkbox"/> 4. E0C60L02 | (Low Power Type <S1C60L02>) | LCD 4.5 V |

### 2. MULTIPLE KEY ENTRY RESET

- COMBINATION .....  1. Not Use
  - 2. Use K00, K01
  - 3. Use K00, K01, K02
  - 4. Use K00, K01, K02, K03

### 3. INTERRUPT NOISE REJECTOR

- K00-K03 .....  1. Use  2. Not Use

### 4. INPUT PORT PULL DOWN RESISTOR

- K00 .....  1. With Resistor  2. Gate Direct
- K01 .....  1. With Resistor  2. Gate Direct
- K02 .....  1. With Resistor  2. Gate Direct
- K03 .....  1. With Resistor  2. Gate Direct

5. R00 SPECIFICATION

- OUTPUT TYPE .....  1. DC Output  
 2. Buzzer Inverted Output (Control bit is R00)  
 3. Buzzer Inverted Output (Control bit is R01)  
 4. FOUT Output
  
- FOUT OUTPUT SPACIFICATION
 

F1 .....	<input type="checkbox"/> 1. 256[Hz]	F3 .....	<input type="checkbox"/> 1. 1,024[Hz]
	<input type="checkbox"/> 2. 512[Hz]		<input type="checkbox"/> 2. 2,048[Hz]
	<input type="checkbox"/> 3. 1,024[Hz]		<input type="checkbox"/> 3. 4,096[Hz]
	<input type="checkbox"/> 4. 2,048[Hz]		<input type="checkbox"/> 4. 8,192[Hz]
	<input type="checkbox"/> 5. 4,096[Hz]		<input type="checkbox"/> 5. 16,384[Hz]
F2 .....	<input type="checkbox"/> 1. 512[Hz]	F4 .....	<input type="checkbox"/> 1. 2,048[Hz]
	<input type="checkbox"/> 2. 1,024[Hz]		<input type="checkbox"/> 2. 4,096[Hz]
	<input type="checkbox"/> 3. 2,048[Hz]		<input type="checkbox"/> 3. 8,192[Hz]
	<input type="checkbox"/> 4. 4,096[Hz]		<input type="checkbox"/> 4. 16,384[Hz]
	<input type="checkbox"/> 5. 8,192[Hz]		<input type="checkbox"/> 5. 32,768[Hz]
  
- OUTPUT SPECIFICATION .....  1. Complementary  2. Pch-OpenDrain

6. R01 SPECIFICATION

- OUTPUT TYPE .....  1. DC Output  2. Buzzer Output
- OUTPUT SPECIFICATION .....  1. Complementary  2. Pch-OpenDrain

7. OUTPUT SPECIFICATION (R02, R03)

- R02 .....  1. Complementary  2. Pch-OpenDrain
- R03 .....  1. Complementary  2. Pch-OpenDrain

8. I/O PORT SPECIFICATION

- P00 .....  1. Complementary  2. Pch-OpenDrain
- P01 .....  1. Complementary  2. Pch-OpenDrain
- P02 .....  1. Complementary  2. Pch-OpenDrain
- P03 .....  1. Complementary  2. Pch-OpenDrain

9. LCD COMMON DUTY AND BIAS

- 1. 1/4 Duty 1/3 Bias
- 2. 1/3 Duty 1/3 Bias
- 3. 1/2 Duty 1/3 Bias
- 4. 1/4 Duty 1/2 Bias
- 5. 1/3 Duty 1/2 Bias
- 6. 1/2 Duty 1/2 Bias

10. OSC1 SYSTEM CLOCK

- 1. Crystal
- 2. CR

### 3.3 Option Specifications and Selection Message

Screen that can be selected as function options set on the S1C60N02 are shown below, and their specifications are also described.

#### 1 Device type and LCD voltage

```

*** OPTION NO.1 ***

--- DEVICE TYPE & LCD POWER VREG ---

      1. E0C6002  LCD 3V
      2. E0C6002  LCD 4.5V
      3. E0C60L02 LCD 3V
      4. E0C60L02 LCD 4.5V

PLEASE SELECT NO.(1) ? 4

      4. E0C60L02 LCD 4.5V  SELECTED
  
```

Select the chip specification.

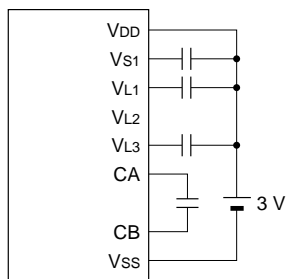
There are two models: E0C6002 (S1C60N02) (3 V supply voltage) and E0C60L02 (S1C60L02) (1.5 V supply voltage, low-power specification).

Select the LCD drive voltage (3 V or 4.5 V) according to the LCD panel to be used.

Figure 3.3.1 shows the external elements.

S1C60N02

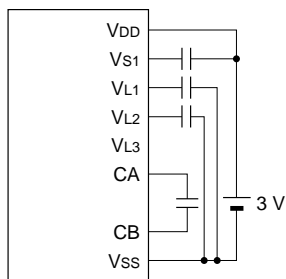
4.5 V LCD panel  
1/4, 1/3, 1/2 duty, 1/3 bias



Note: VL2 is shorted to VSS inside the IC.

S1C60N02

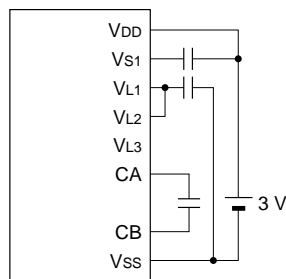
3 V LCD panel  
1/4, 1/3, 1/2 duty, 1/3 bias



Note: VL3 is shorted to VSS inside the IC.

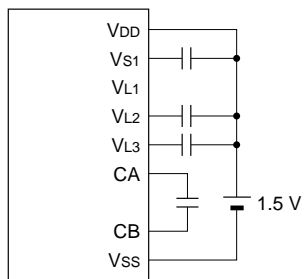
S1C60N02

3 V LCD panel  
1/4, 1/3, 1/2 duty, 1/2 bias



S1C60L02

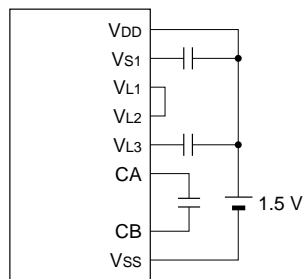
4.5 V LCD panel  
1/4, 1/3, 1/2 duty, 1/3 bias



Note: VL1 is shorted to VSS inside the IC.

S1C60L02

3 V LCD panel  
1/4, 1/3, 1/2 duty, 1/2 bias



Note: VL1 is shorted to VSS inside the IC.

Fig. 3.3.1 External elements

## 2 Multiple key entry reset

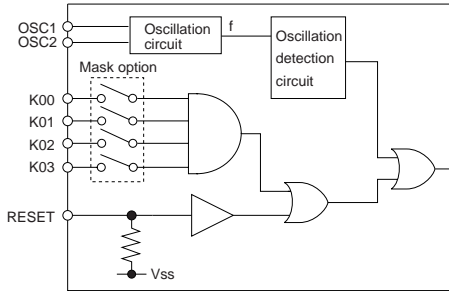
```

*** OPTION NO.2 ***
--- MULTIPLE KEY ENTRY RESET ---

COMBINATION      1. NOT USE
                  2. USE K00,K01
                  3. USE K00,K01,K02
                  4. USE K00,K01,K02,K03

PLEASE SELECT NO.(1) ? 2 [ ]

COMBINATION      2. USE K00,K01  SELECTED
    
```



The reset function is set when K00 through K03 are entered.

When "NOT USE" is selected, the reset function is not activated even if K00 through K03 are entered. When "USE K00, K01" is selected, the system is reset immediately the K00 and K01 inputs go high at the same time. Similarly, the system is reset as soon as the K00 through K02 inputs or the K00 through K03 inputs go high.

However, the system is reset when a high signal is input for more than a rule time (1–3 sec).

The system reset circuit is shown in Figure 3.3.2.

Fig. 3.3.2  
System reset circuit

## 3 Interrupt noise rejector

```

*** OPTION NO.3 ***
--- INTERRUPT NOISE REJECTOR ---

K00-K03          1. USE
                  2. NOT USE

PLEASE SELECT NO.(1) ? 1 [ ]

K00-K03          1. USE  SELECTED
    
```

Select whether noise rejector will be supplemented to the input interrupter of K00–K03. When "USE" is selected, the entry signal will pass the noise rejector, and occurrence of interrupt errors due to noise or chattering can be avoided. Note, however, that because the noise rejector performs entry signal sampling at 4 kHz, "NOT USE" should be selected when high speed response is required.

## 4 Input ports pull down resistor

```

*** OPTION NO.4 ***
--- INPUT PORT PULL DOWN RESISTOR ---

K00              1. WITH RESISTOR
                  2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1 [ ]

K01              1. WITH RESISTOR
                  2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1 [ ]

K02              1. WITH RESISTOR
                  2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1 [ ]

K03              1. WITH RESISTOR
                  2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1 [ ]

K00              1. WITH RESISTOR  SELECTED
K01              1. WITH RESISTOR  SELECTED
K02              1. WITH RESISTOR  SELECTED
K03              1. WITH RESISTOR  SELECTED
    
```

Select whether input ports (K00–K03) will each be supplemented with pull down resistors or not.

When "GATE DIRECT" is selected, see to it that entry floating state does not occur. Select "WITH RESISTOR" pull down resistor for unused ports. Moreover, the input port status is changed from "H" level (VDD) to "L" (VSS) with pull down resistors, a delay of approximately 1 msec in waveform rise time will occur depending on the pull down resistor and entry load time constant. Because of this, when input reading is to be conducted, ensure the appropriate wait time with the program.

The configuration of the pull down resistor circuit is shown in Figure 3.3.3.

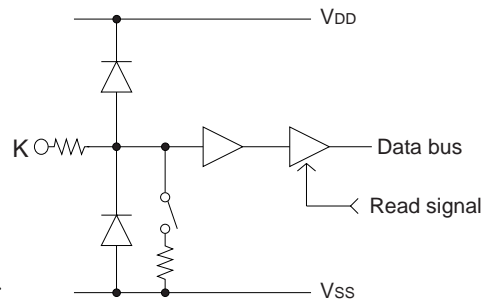


Fig. 3.3.3  
Configuration of pull down resistor

## 5 R00 specification

```

*** OPTION NO.5 ***

--- R00 SPECIFICATION ---

      OUTPUT TYPE          1. DC
                          2. /BZ OUTPUT R00
                          3. /BZ OUTPUT R01
                          4. FOUT

PLEASE SELECT NO.(4) ? 4 

      F1                   1. 256 [HZ]
                          2. 512 [HZ]
                          3. 1024 [HZ]
                          4. 2048 [HZ]
                          5. 4096 [HZ]

PLEASE SELECT NO.(4) ? 4 

      F2                   1. 512 [HZ]
                          2. 1024 [HZ]
                          3. 2048 [HZ]
                          4. 4096 [HZ]
                          5. 8192 [HZ]

PLEASE SELECT NO.(4) ? 4 

      F3                   1. 1024 [HZ]
                          2. 2048 [HZ]
                          3. 4096 [HZ]
                          4. 8192 [HZ]
                          5. 16384 [HZ]

PLEASE SELECT NO.(4) ? 4 

      F4                   1. 2048 [HZ]
                          2. 4096 [HZ]
                          3. 8192 [HZ]
                          4. 16384 [HZ]
                          5. 32768 [HZ]

PLEASE SELECT NO.(4) ? 4 

      OUTPUT SPECIFICATION 1. COMPLEMENTARY
                          2. PCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1 

      OUTPUT TYPE          4. FOUT      SELECTED
      F1                   4. 2048 [HZ] SELECTED
      F2                   4. 4096 [HZ] SELECTED
      F3                   4. 8192 [HZ] SELECTED
      F4                   4. 16384 [HZ] SELECTED
      OUTPUT SPECIFICATION 1. COMPLEMENTARY SELECTED
  
```

Select the output specification for R00 terminal. Either complementary output or Pch open drain output may be selected. When "DC" (DC output) is selected, R00 becomes a regular output port. When "/BZ OUTPUT R00" (buzzer inverted output, control bit is R00) is selected, by writing "1" to the R00 register, clock with frequency specified through the software is generated from R00 terminal. When "/BZ OUTPUT R01" (buzzer inverted output, control bit is R01) is selected, by writing "1" to the R01 register, clock with frequency specified through the software is generated from R00 terminal. When FOUT is selected, clock with frequency selected from R00 terminal is generated by writing "1" to the R00 register. When the DC output or buzzer inverted output is selected as the output type, the FOUT frequencies cannot be selected.

- When DC output is selected  
When R00 register (F3 address, D0 bit) is set to "1", the R00 terminal output goes high (VDD), and goes low (VSS) when set to "0".  
Output waveform is shown in Figure 3.3.4.
- When buzzer inverted output (control bit is R00) is selected  
When R00 register is set to "1", 50% duty and VDD-VSS amplitude square wave is generated at the specified frequency by the software. When set to "0", R00 terminal goes low (VSS). The clock phase when buzzer drive signal is output from R00 terminal is antiphase to that of R01 terminal.  
Output waveform is shown in Figure 3.3.5.
- When buzzer inverted output (control bit is R01) is selected  
When R01 register is set to "1", 50% duty and VDD-VSS amplitude square wave is generated at the specified frequency by the software. When set to "0", R00 terminal goes low (VSS). The clock phase when buzzer drive signal is output from R00 terminal is antiphase to that of R01 terminal.  
Output waveform is shown in Figure 3.3.5.

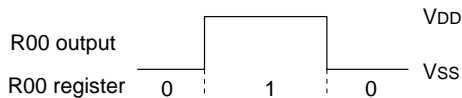


Fig. 3.3.4 Output waveform at DC output selection

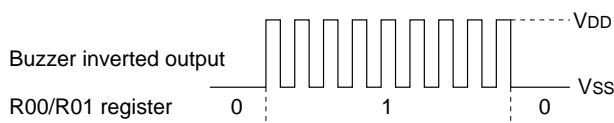


Fig. 3.3.5 Output waveform at buzzer inverted output selection

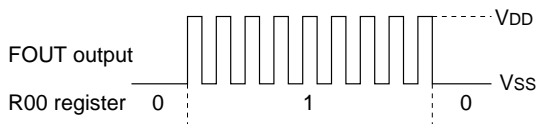


Fig. 3.3.6 Output waveform at FOUT output selection

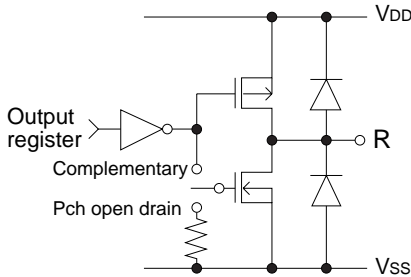


Fig. 3.3.7 Configuration of output circuit

- When FOUT output is selected  
When R00 register is set to "1", 50% duty and VDD–VSS amplitude square wave is generated at the specified frequency. When set to "0", the FOUT terminal goes low (VSS).  
The F1 to F4 FOUT frequencies are set by mask option. One of them is used by the software.  
FOUT output is normally utilized to provide clock to other devices but since hazard occurs at the square wave breaks, great caution must be observed when using it.  
Output waveform is shown in Figure 3.3.6.

The output circuit configuration is shown in Figure 3.3.7.

### 6 R01 specification

```

*** OPTION NO.6 ***
--- R01 SPECIFICATION ---
    OUTPUT TYPE          1. DC
                        2. BZ OUTPUT
PLEASE SELECT NO.(1) ? 2 
    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                        2. PCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1 
    OUTPUT TYPE          2. BZ OUTPUT  SELECTED
    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    
```

Select the output specification for R01 terminal. Either complementary output or Pch open drain output may be selected. When "DC" (DC output) is selected, R01 becomes a regular output port. When "BZ OUTPUT" (buzzer output) is selected, by writing "1" to the R01 register, clock with frequency specified through the software is generated from R01 terminal.



Fig. 3.3.8 Output waveform at DC output selection

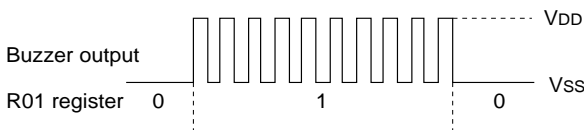


Fig. 3.3.9 Output waveform at buzzer output selection

- When DC output is selected  
When R01 register (F3 address, D1 bit) is set to "1", the R01 terminal output goes high (VDD), and goes low (VSS) when set to "0".  
Output waveform is shown in Figure 3.3.8.
- When buzzer output is selected  
When R01 register is set to "1", 50% duty and VDD–VSS amplitude square wave is generated at the specified frequency by the software. When set to "0", R01 terminal goes low (VSS). The clock phase when buzzer drive signal is output from R01 terminal is antiphase to that of R00 terminal.  
Output waveform is shown in Figure 3.3.9.

### 7 Output port output specification (R02, R03)

```

*** OPTION NO.7 ***
--- OUTPUT PORT SPECIFICATION ---
      R02                1. COMPLEMENTARY
                        2. PCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 2 [ ]

      R03                1. COMPLEMENTARY
                        2. PCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 2 [ ]

      R02                2. PCH-OPENDRAIN   SELECTED
      R03                2. PCH-OPENDRAIN   SELECTED
    
```

Select the output specification for R02 and R03 output ports. Either complementary output or Pch open drain output may be selected. When output port is to be used on key matrix configuration, select Pch open drain output. For unused output ports, select complementary output. The circuit configuration is the same as that of output ports (R00 shown in Figure 3.3.7).

### 8 I/O port specification

```

*** OPTION NO.8 ***
--- I/O PORT OUTPUT SPECIFICATION ---
      P00                1. COMPLEMENTARY
                        2. PCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 2 [ ]

      P01                1. COMPLEMENTARY
                        2. PCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 2 [ ]

      P02                1. COMPLEMENTARY
                        2. PCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 2 [ ]

      P03                1. COMPLEMENTARY
                        2. PCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 2 [ ]

      P00                2. PCH-OPENDRAIN   SELECTED
      P01                2. PCH-OPENDRAIN   SELECTED
      P02                2. PCH-OPENDRAIN   SELECTED
      P03                2. PCH-OPENDRAIN   SELECTED
    
```

Select the output specification to be used during I/O ports (P00–P03) output mode selection. Either complementary output or Pch open drain output may be selected. The circuit configuration of the output driver is the same as that of output ports (R00 shown in Figure 3.3.7). Select complementary output for unused ports. The I/O ports can control the input/output direction according to the IOC bit (FC address, D0 bit); at "1" and "0" settings, it is set to output port and input port, respectively. The pull down resistor of this port is turned on by the read signal and is normally turned off to minimize leak current. Because of this, when the port is set for input, take care that a floating state does not occur in the terminal. The circuit configuration of the I/O port is shown in Figure 3.3.10.

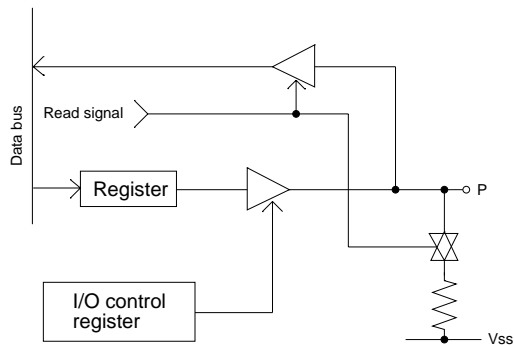


Fig. 3.3.10 Configuration of I/O port

9 LCD common duty and bias

```

*** OPTION NO.9 ***

--- LCD COMMON DUTY AND BIAS ---

1. 1/4 DUTY 1/3 BIAS
2. 1/3 DUTY 1/3 BIAS
3. 1/2 DUTY 1/3 BIAS
4. 1/4 DUTY 1/2 BIAS
5. 1/3 DUTY 1/2 BIAS
6. 1/2 DUTY 1/2 BIAS

PLEASE SELECT NO.(1) ? 1 [ ]

1. 1/4 DUTY 1/3 BIAS  SELECTED
    
```

Table 3.3.1 Common duty selection standard

Number of segments	Common duty
1-40	1/2
41-60	1/3
61-80	1/4

Select the common (drive) duty and bias. When 1/2 duty is selected, up to 40 segments of LCD panel can be driven with 2 COM terminals and 20 SEG terminals. When 1/3 duty is selected, up to 60 segments can be driven with 3 COM terminals, and when 1/4 duty is selected, up to 80 segments with 4 COM terminals. When 1/2 duty is selected, the COM0 and COM1 terminals are effective for COM output and the COM2 and COM3 terminals always output an off signal. When 1/3 duty is selected, the COM0 to COM2 terminals are effective and the COM3 terminal always outputs an off signal. Refer to Table 3.3.1 for common duty selection.

For the LCD drive bias, either 1/3 bias (drives LCD with 4 levels, VDD, VL1, VL2 and VL3) or 1/2 bias (drives LCD with 3 levels, VDD, VL1=VL2 and VL3) can be selected.

By selecting 1/2 bias, external elements can be minimized (see Figure 3.3.1). Furthermore, when 1/2 bias is selected, be sure to short between the VL1 terminal and the VL2 terminal outside the IC. Figures 3.3.11 and 3.3.12 show the drive waveforms of 1/3 bias driving and 1/2 bias driving, respectively.

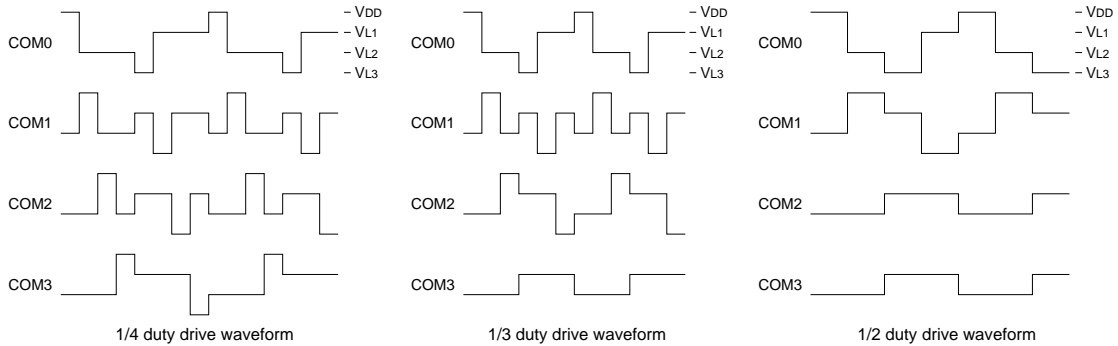


Fig. 3.3.11 Drive waveform from COM terminals (1/3 bias)

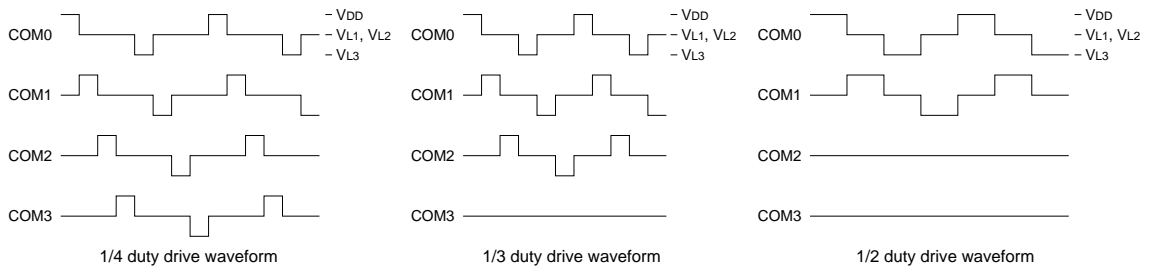


Fig. 3.3.12 Drive waveform from COM terminals (1/2 bias)

**10 OSC1 system clock**

```

*** OPTION NO.10 ***
--- OSC1 SYSTEM CLOCK ---
                                1. CRYSTAL
                                2. CR
PLEASE SELECT NO.(1) ? 1 
                                1. CRYSTAL  SELECTED

```

Select oscillation circuit that uses OSC1 and OSC2 for the S1C60N02/60L02.

To minimize external components, CR oscillation circuit would be suitable; to obtain a stable oscillation frequency, crystal oscillation circuit would be suitable.

When CR oscillation circuit is selected, only resistors are needed as external components since capacities are built-in.

On the other hand, when crystal oscillation circuit is selected, crystal oscillator and trimmer capacitor are needed as external components. Although when crystal oscillation circuit is selected, it is fixed at 32.768 kHz, when CR oscillation circuit is selected, frequency may be modified to a certain extent depending on the resistance of external components.

## 3.4 FOG6002 Quick Reference

### ■ Starting command and input/output files

**Execution file:** FOG6002.EXE

**Starting command:** FOG6002

indicates the Return key.

**Input file:** C002XXXF.DOC (Function option document file, when modifying)

**Output file:** C002XXXF.DOC (Function option document file)  
C002XXXF.HEX (Function option HEX file)

### ■ Display example

```

*** E0C6002 FUNCTION OPTION GENERATOR. --- Ver 3.00 ***
EEEEEEEEEE PPPPPPPP SSSSSSS 0000000 NNN NNN
EEEEEEEEEE PPPPPPPP SSS SSSS 000 000 NNNN NNN
EEE PPP PPP SSS SSS 000 000 NNNNN NNN
EEE PPP PPP SSS 000 000 NNNNNN NNN
EEEEEEEEEE PPPPPPPP SSSSSSS 000 000 NNN NNN NNN
EEEEEEEEEE PPPPPPPP SSSS 000 000 NNN NNNNNN
EEE PPP SSS 000 000 NNN NNNNNN
EEE PPP SSS SSS 000 000 NNN NNNN
EEEEEEEEEE PPP SSSS SSS 000 000 NNN NNN
EEEEEEEEEE PPP SSSSSSS 0000000 NNN NN

(C) COPYRIGHT 1991 SEIKO EPSON CORP.

THIS SOFTWARE MAKES NEXT FILES.

C002XXXF.HEX ... FUNCTION OPTION HEX FILE.
C002XXXF.DOC ... FUNCTION OPTION DOCUMENT FILE.

STRIKE ANY KEY.
```

#### Start-up message

When FOG6002 is started, the start-up message is displayed.

For "STRIKE ANY KEY.", press any key to advance the program execution.

To suspend execution, press the "CTRL" and "C" keys together: the sequence returns to the DOS command level.

```

*** E0C6002 USER'S OPTION SETTING. --- Ver 3.00 ***
CURRENT DATE IS 97/02/03
PLEASE INPUT NEW DATE : 
```

#### Date input

Enter the 2-digit year, month, and day of the month by delimiting them with a slash ("/").

When not modifying the date, press the RETURN key "" to continue.

```

*** OPERATION SELECT MENU ***
1. INPUT NEW FILE
2. EDIT FILE
3. RETURN TO DOS

PLEASE SELECT NO.?
```

#### Operation selection menu

Enter a number from 1 to 3 to select a subsequent operation.

1. To set new function options.
2. To modify the document file.
3. To terminate FOG6002.

```

*** OPERATION SELECT MENU ***
1. INPUT NEW FILE
2. EDIT FILE
3. RETURN TO DOS

PLEASE SELECT NO.? 1 
PLEASE INPUT FILE NAME? C0020A0  .. (1)
PLEASE INPUT USER'S NAME? SEIKO EPSON CORP.  .. (2)
PLEASE INPUT ANY COMMENT
(ONE LINE IS 50 CHR)? ED MARKETING DEPARTMENT  .. (3)
? 421-8 HINO HINO-SHI TOKYO 191-8501 JAPAN 
? TEL 042-587-5816 
? FAX 042-587-5624 
? 
```

#### Setting new function options

Select "1" on the operation selection menu.

- (1) Enter the file name.
- (2) Enter the customer's company name.
- (3) Enter any comment.

(Within 50 characters x 10 lines)

Next, start function option setting from option No. 1.

In case a function option document file with the same name as the file name specified in the current drive exists, the user is asked whether overwriting is desired. Enter "Y" or "N" accordingly.

```

PLEASE INPUT FILE NAME? C0020A0 
EXISTS OVERWRITE(Y/N)? N 
PLEASE INPUT FILE NAME? C0020B0 
PLEASE INPUT USER'S NAME?
```

```

*** OPERATION SELECT MENU ***

    1. INPUT NEW FILE
    2. EDIT FILE
    3. RETURN TO DOS

PLEASE SELECT NO.? 2 [ ]

*** SOURCE FILE(S) ***

C0020A0          C0020B0          C0020C0          ..(1)

PLEASE INPUT FILE NAME? C0020A0 [ ] ..(2)
PLEASE INPUT USER'S NAME? [ ] ..(3)
PLEASE INPUT ANY COMMENT
(ONE LINE IS 50 CHR)? [ ] ..(4)
PLEASE INPUT EDIT NO.? 4 [ ] ..(5)
:
:
(Modifying function option settings)
:
PLEASE INPUT EDIT NO.? E [ ]

```

In step (1), if no modifiable source exists, the following message is displayed and the sequence returns to the operation selection menu.

```

*** SOURCE FILE(S) ***

FUNCTION OPTION DOCUMENT FILE IS NOT FOUND.

```

In step (2), if the function option document file is not in the current drive, the following message is displayed, prompting entry of other file name.

```

PLEASE INPUT FILE NAME? C0020N0 [ ]
FUNCTION OPTION DOCUMENT FILE IS NOT FOUND.
PLEASE INPUT FILE NAME?

```

```

*** OPTION NO.2 ***

--- MULTIPLE KEY ENTRY RESET ---

COMBINATION      1. Not Use
                  2. Use   K00,K01
                  3. Use   K00,K01,K02
                  4. Use   K00,K01,K02,K03

PLEASE SELECT NO.(1) ? 2 [ ]

COMBINATION      2. Use   K00,K01  SELECTED

```

```

END OF OPTION SETTING.
DO YOU MAKE HEX FILE (Y/N) ? Y [ ] ..(1)

*** OPTION EPROM SELECT MENU ***

    1. 27C64
    2. 27C128
    3. 27C256
    4. 27C512

PLEASE SELECT NO.? 2 [ ] ..(2)

    2. 27C128  SELECTED

MAKING FILE(S) IS COMPLETED.

*** OPERATION SELECT MENU ***

    1. INPUT NEW FILE
    2. EDIT FILE
    3. RETURN TO DOS

PLEASE SELECT NO.?

```

### Modifying function option settings

Select "2" on the operation selection menu.

- (1) Will display the files on the current drive.
- (2) Enter the file name.
- (3) Enter the customer's company name.
- (4) Enter any comment.

Previously entered data can be used by pressing the RETURN key "[ ]" at (3) and (4).

- (5) Enter the number of the function option to be modified. When selection of one option is complete, the system prompts entry of another function option number. Repeat selection until all options to be modified are selected. Enter "E [ ]" to end option setting. Then, move to the confirmation procedure for HEX file generation.

### Option selection

The selections for each option correspond one to one to the option list. Enter the selection number. The value in parentheses ( ) indicates the default value, and is set when only the RETURN key "[ ]" is pressed.

In return, the confirmation is displayed.

When you wish to modify previously set function options in the new setting process, enter "B [ ]" to return 1 step back to the previous function option setting operation.

### EPROM selection

When setting function options setting is completed, the following message is output to ask the operator whether to generate the HEX file.

- (1) When debugging the program with the evaluation board, HEX file is needed, so enter "Y [ ]". If "N [ ]" is entered, no HEX file is generated and only document file is generated.
- (2) For the option ROM selection menu displayed when "Y [ ]" is entered in Step (1), select the EPROM to be used for setting evaluation board options.

When a series of operations are complete, the sequence returns to the operation selection menu.

## 3.5 Sample File

### ■ Example of function option document file

```

* E0C6002 FUNCTION OPTION DOCUMENT V 3.00
*
* FILE NAME      C0020A0F.DOC
* USER'S NAME   SEIKO EPSON CORP.
* INPUT DATE    97/02/03
*
* COMMENT       ED MARKETING DEPARTMENT
*               421-8 HINO HINO-SHI TOKYO 191-8501 JAPAN
*               TEL 042-587-5816
*               FAX 042-587-5624
*
*
* OPTION NO.1
* < DEVICE TYPE & LCD POWER VREG >
*               E0C60L02 LCD 4.5V ----- SELECTED
OPT0101 02
OPT0103 03
*
* OPTION NO.2
* < MULTIPLE KEY ENTRY RESET >
*   COMBINATION   USE  K00,K01 ----- SELECTED
OPT0201 02
*
* OPTION NO.3
* < INTERRUPT NOISE REJECTOR >
*   K00-K03      USE  ----- SELECTED
OPT0301 01
*
* OPTION NO.4
* < INPUT PORT PULL DOWN RESISTOR >
*   K00          WITH RESISTOR ----- SELECTED
*   K01          WITH RESISTOR ----- SELECTED
*   K02          WITH RESISTOR ----- SELECTED
*   K03          WITH RESISTOR ----- SELECTED
OPT0401 01
OPT0402 01
OPT0403 01
OPT0404 01
*
* OPTION NO.5
* < R00 SPECIFICATION >
*   OUTPUT TYPE  FOUT ----- SELECTED
*   F1          2048 (HZ) ----- SELECTED
*   F2          4096 (HZ) ----- SELECTED
*   F3          8192 (HZ) ----- SELECTED
*   F4          16384 (HZ) ----- SELECTED
*   OUTPUT SPECIFICATION  COMPLEMENTARY ----- SELECTED
OPT0501 04
OPT0503 04
OPT0504 04
OPT0505 04
OPT0506 04
OPT0507 01
*
* OPTION NO.6
* < R01 PORT OUTPUT SPECIFICATION >
*   OUTPUT TYPE  BZ OUTPUT ----- SELECTED
*   OUTPUT SPECIFICATION  COMPLEMENTARY ----- SELECTED
OPT0601 02
OPT0602 01
*
* OPTION NO.7
* < OUTPUT PORT SPECIFICATION R02,R03 >
*   R02          PCH-OPENDRAIN ----- SELECTED
*   R03          PCH-OPENDRAIN ----- SELECTED
OPT0701 02
OPT0702 02

```

```

*
* OPTION NO.8
* < I/O PORT OUTPUT SPECIFICATION >
*   P00                PCH-OPENDRAIN  -----  SELECTED
*   P01                PCH-OPENDRAIN  -----  SELECTED
*   P02                PCH-OPENDRAIN  -----  SELECTED
*   P03                PCH-OPENDRAIN  -----  SELECTED
OPT0801 02
OPT0802 02
OPT0803 02
OPT0804 02
*
* OPTION NO.9
* < LCD COMMON DUTY AND BIAS >
*   1/4 DUTY 1/3 BIAS  -----  SELECTED
OPT0901 01
*
* OPTION NO.10
* < OSC 1 SYSTEM CLOCK >
*   CRYSTAL  -----  SELECTED
OPT1001 01
*
*
* SEIKO EPSON'S AREA
*
*
* OPTION NO.11
OPT1101 01
OPT1102 01
OPT1103 01
OPT1104 01
*
* OPTION NO.12
OPT1201 02
OPT1202 02
OPT1203 02
OPT1204 02
*
* OPTION NO.13
OPT1301 01
\\END

```

*Note End mark "¥END" may be used instead of "\\END" depending on the PC used. (The code of \ and ¥ is 5CH.)*

# 4 SEGMENT OPTION GENERATOR SOG6002

## 4.1 SOG6002 Outline

With the 4-bit single-chip S1C60N02 microcomputers, the customer may select the LCD segment options. By modifying the mask patterns of the S1C60N02 according to the selected options, the system can be customized to meet the specifications of the target system. The Segment Option Generator SOG6002 is a software tool for generating data file used to generate mask patterns. From the data file created with SOG6002, the S1C60N02 mask pattern is automatically generated by a general purpose computer. The HEX file for the evaluation board (S5U1C62N51E1) segment option ROM is simultaneously generated with the data file.

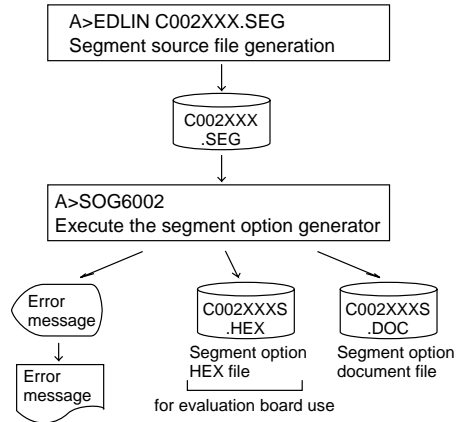


Fig. 4.1.1 SOG6002 execution flow

The operating method is same as for the S1C62 Family. Refer to the "S1C62 Family Development Tool Reference Manual" for details.

## 4.2 Option List

TERMINAL NAME	ADDRESS												OUTPUT SPECIFICATION	
	COM0			COM1			COM2			COM3				
	H	L	D	H	L	D	H	L	D	H	L	D		
SEG0														SEG output
SEG1														DC output <input type="checkbox"/> C <input type="checkbox"/> P
SEG2														SEG output
SEG3														DC output <input type="checkbox"/> C <input type="checkbox"/> P
SEG4														SEG output
SEG5														DC output <input type="checkbox"/> C <input type="checkbox"/> P
SEG6														SEG output
SEG7														DC output <input type="checkbox"/> C <input type="checkbox"/> P
SEG8														SEG output
SEG9														DC output <input type="checkbox"/> C <input type="checkbox"/> P
SEG10														SEG output
SEG11														DC output <input type="checkbox"/> C <input type="checkbox"/> P
SEG12														SEG output
SEG13														DC output <input type="checkbox"/> C <input type="checkbox"/> P
SEG14														SEG output
SEG15														DC output <input type="checkbox"/> C <input type="checkbox"/> P
SEG16														SEG output
SEG17														DC output <input type="checkbox"/> C <input type="checkbox"/> P
SEG18														SEG output
SEG19														DC output <input type="checkbox"/> C <input type="checkbox"/> P
Legend:	<ADDRESS> H: High order address, L: Low order address D: Data bit												<OUTPUT SPECIFICATION> C: Complementary output P: Pch open drain output	

### 4.3 Segment Ports Output Specifications

For the output specification of the segment output ports (SEG0–SEG19), segment output and DC output can be selected in units of two terminals. When used for liquid crystal panel drives, select segment output; when used as regular output port, select DC output. When DC output is selected, either complementary output or Pch open drain output may further be selected.

However, for segment output ports that will not be used, select segment output.

Refer to the "S1C62 Family Development Tool Reference Manual" for the segment option source file creation.

#### ■ When segment output is selected

The segment output port has a segment decoder built-in, and the data bit of the optional address in the segment memory area (090H–0AFH) can be allocated to the optional segment. With this, up to 80 segments (60 segments when 1/3 duty is selected and 40 segments when 1/2 duty is selected) of liquid crystal panel could be driven.

The segment memory may be allocated only one segment and multiple setting is not possible.

The allocated segment displays when the bit for this segment memory is set to "1", and goes out when bit is set to "0".

Segment allocation is set to H for high address (9–A), to L for low address (0–F), and to D for data bit (0–3) and are recorded in their respective column in the option list. For segment ports that will not be used, write "---" (hyphen) in the H, L, and D columns of COM0–COM3.

Examples

- When 1/4 duty is selected

```
0 901 900 932 903 S
1 912 911 910 923 S
```

- When 1/3 duty is selected

```
0 901 900 932 --- S
1 912 911 910 --- S
```

- When 1/2 duty is selected

```
0 901 900 --- --- S
1 912 911 --- --- S
```

#### ■ When DC output is selected

The DC output can be selected in units of two terminals and up to 20 terminals may be allocated for DC output. Also, either complementary output or Pch open drain output is likewise selected in units of two terminals. When the bit for the selected segment memory is set to "1", the segment output port goes high (VDD), and goes low (VSS) when set to "0". Segment allocation is the same as when segment output is selected but for the while the segment memory allocated to COM1–COM3 becomes ineffective. Write three hyphens ("---") in the COM1–COM3 columns in the option list.

Example

- When complementary output is set to SEG16 and SEG17, and Pch open drain output is set to SEG18 and SEG19.

```
16 AE0 --- --- --- C
17 AF0 --- --- --- C
18 AE1 --- --- --- P
19 AF1 --- --- --- P
```

*Note* Only complementary output is enabled as the DC output of the SEG ports of the evaluation board. Therefore, complementary output is enabled even if Pch open drain output is selected. Respond to it by adding external circuits as required.

## 4.4 SOG6002 Quick Reference

### ■ Starting command and input/output files

**Execution file:** SOG6002.EXE

\_ indicates a blank.

indicates the Return key.

A parameter enclosed by [ ] can be omitted.

**Starting command:** SOG6002\_ [-H]

**Option:** -H: Specifies the segment option document file for input file of SOG6002.

**Input file:** C002XXX.SEG (Segment option source file)  
C002XXXS.DOC (Segment option document file, when -H option use)

**Output file:** C002XXXS.DOC (Segment option document file)  
C002XXXS.HEX (Segment option HEX file)

### ■ Display example

```

*** E0C6002 SEGMENT OPTION GENERATOR. --- Ver 3.00 ***
EEEEEEEEEE PPPPPPPP SSSSSSS 00000000 NNN NNN
EEEEEEEEEE PPPPPPPP SSS SSS 000 000 NNNN NNN
EEE PPP PPP SSS SSS 000 000 NNNNN NNN
EEE PPP PPP SSS 000 000 NNNNNN NNN
EEEEEEEEEE PPPPPPPP SSSSSSS 000 000 NNN NNN NNN
EEEEEEEEEE PPPPPPPP SSSSS 000 000 NNN NNNNNN
EEE PPP SSS SSS 000 000 NNN NNNN
EEE PPP SSS SSS 000 000 NNN NNNN
EEEEEEEEEE PPP SSS SSS 000 000 NNN NNN
EEEEEEEEEE PPP SSSSSSS 00000000 NNN NN
(C) COPYRIGHT 1991 SEIKO EPSON CORP.
SEGMENT OPTION SOURCE FILE NAME IS " C002XXX.SEG "
THIS SOFTWARE MAKES NEXT FILES.
C002XXXS.HEX ... SEGMENT OPTION HEX FILE.
C002XXXS.DOC ... SEGMENT OPTION DOCUMENT FILE.
STRIKE ANY KEY.

```

#### Start-up message

When SOG6002 is started, the start-up message is displayed.

For "STRIKE ANY KEY.", press any key to advance the program execution.

To suspend execution, press the "CTRL" and "C" keys together: the sequence returns to the DOS command level.

```

*** E0C6002 USER'S OPTION SETTING. --- Ver 3.00 ***
CURRENT DATE IS 97/02/03
PLEASE INPUT NEW DATE : 

```

#### Date input

Enter the 2-digit year, month, and day of the month by delimiting them with a slash ("/").

When not modifying the date, press the RETURN key "" to continue.

```

*** SOURCE FILE(S) ***
C0020A0 C0020B0 C0020C0 ..(1)
PLEASE INPUT SEGMENT OPTION FILE NAME? C0020A0 ..(2)
PLEASE INPUT USER'S NAME? SEIKO EPSON CORP. ..(3)
PLEASE INPUT ANY COMMENT
(ONE LINE IS 50 CHR)? ED MARKETING DEPARTMENT ..(4)
? 421-8 HINO HINO-SHI TOKYO 191-8501 JAPAN
? TEL 042-587-5816
? FAX 042-587-5624


```

#### Input file selection

- (1) Will display the files on the current drive.
- (2) Enter the file name.
- (3) Enter the customer's company name.
- (4) Enter any comment.

(Within 50 characters x 10 lines)

Then, move to the confirmation procedure for HEX file generation.

```

*** SOURCE FILE(S) ***
SEGMENT OPTION SOURCE FILE IS NOT FOUND. ..(5) -H option not use
*** SOURCE FILE(S) ***
SEGMENT OPTION DOCUMENT FILE IS NOT FOUND. ..(6) -H option use

```

In step (1), if no modifiable source exists, an error message (5) or (6) will be displayed and the program will be terminated.

In step (2), if the specified file name is not found in the current drive, an error message (7) or (8) is displayed, prompting entry of other file name.

```

PLEASE INPUT SEGMENT OPTION SOURCE FILE NAME? C0020N0
SEGMENT OPTION SOURCE FILE IS NOT FOUND. ..(7) -H option not use
PLEASE INPUT SEGMENT OPTION DOCUMENT FILE NAME? C0020N0
SEGMENT OPTION DOCUMENT FILE IS NOT FOUND. ..(8) -H option use

```

```

END OF OPTION SETTING.
DO YOU MAKE HEX FILE (Y/N) ? Y  ..(1)

*** OPTION EPROM SELECT MENU ***

    1. 27C64
    2. 27C128
    3. 27C256
    4. 27C512

PLEASE SELECT NO.? 2  ..(2)

    2. 27C128   SELECTED

MAKING FILE IS COMPLETED.

```

**EPROM selection**

When selecting file is completed, the following message is output to ask the operator whether to generate the HEX file.

- (1) When debugging the program with the evaluation board, HEX file is needed, so enter "Y ". If "N " is entered, no HEX file is generated and only document file is generated.
- (2) For the option ROM selection menu displayed when "Y " is entered in Step (1), select the EPROM to be used for setting evaluation board options.

When a series of operations are complete, the SOG6002 generates files. If no error is committed while setting segment options, "MAKING FILE IS COMPLETED" will be displayed and the SOG6002 program will be terminated.

**■ Error messages**

Error message	Explanation
S (Syntax Error)	The data was written in an invalid format.
N (Segment No. Select Error)	The segment number outside the specificable range was specified.
R (RAM Address Select Error)	The segment memory address or data bit outside the specificable range was specified.
D (Duprication Error)	The same data (SEG port No., segment memory address, or data bit) was specified more then once.
Out Port Set Error	The output specifications were not set in units of two ports.

## 4.5 Sample Files

---

### ■ Example of segment option source file

```
; C0020A0.SEG, VER.3.00
; LCD SEGMENT DECODE TABLE
;
0  900  901  902  903  S
1  910  911  912  913  S
2  920  921  922  923  S
3  930  931  932  933  S
4  940  941  942  943  S
5  950  951  952  953  S
6  960  961  962  963  S
7  970  971  972  973  S
8  980  981  982  983  S
9  990  991  992  993  S
10 9A0  9A1  9A2  9A3  S
11 9B0  9B1  9B2  9B3  S
12 9C0  9C1  9C2  9C3  S
13 9D0  9D1  9D2  9D3  S
14 9E0  9E1  9E2  9E3  S
15 9F0  9F1  9F2  9F3  S
16 A00  A01  A02  A03  S
17 A10  A11  A12  A13  S
18 A20  ---  ---  ---  C
19 A30  ---  ---  ---  C
```

### ■ Example of segment option document file

```
* E0C6002 SEGMENT OPTION DOCUMENT V 3.00
*
* FILE NAME      C0020A0S.DOC
* USER'S NAME    SEIKO EPSON CORP.
* INPUT DATE     97/02/03
* COMMENT        ED MARKETING DEPARTMENT
*                421-8 HINO HINO-SHI TOKYO 191-8501 JAPAN
*                TEL 042-587-5816
*                FAX 042-587-5624
*
*
* OPTION NO.17
*
* < LCD SEGMENT DECODE TABLE >
*
* SEG COM0 COM1 COM2 COM3 SPEC
*
0  900  901  902  903  S
1  910  911  912  913  S
2  920  921  922  923  S
3  930  931  932  933  S
4  940  941  942  943  S
5  950  951  952  953  S
6  960  961  962  963  S
7  970  971  972  973  S
8  980  981  982  983  S
9  990  991  992  993  S
10 9A0  9A1  9A2  9A3  S
11 9B0  9B1  9B2  9B3  S
12 9C0  9C1  9C2  9C3  S
13 9D0  9D1  9D2  9D3  S
14 9E0  9E1  9E2  9E3  S
15 9F0  9F1  9F2  9F3  S
16 A00  A01  A02  A03  S
17 A10  A11  A12  A13  S
18 A20  A21  A22  A23  C
19 A30  A31  A32  A33  C
\\END
```

Note End mark "¥¥END" may be used instead of "\\END" depending on the PC used. (The code of \ and ¥ is 5CH.)

# 5 ICE CONTROL SOFTWARE ICS6002

## 5.1 ICS6002 Outline

The In-Circuit Emulator (S5U1C62000H) connects the target board produced by the user via the evaluation board (S5U1C62N51E1) and performs real time target system evaluation and debugging by passing through the RS-232C from the host computer and controlling it. The operation on the host computer side and ICE (S5U1C62000H) control is done through the ICE Control Software ICS6002.

The ICS6002 has a set of numerous and highly functional emulation commands which provide sophisticated break function, on-the-fly data display, history display, etc., and so perform a higher level of debugging.

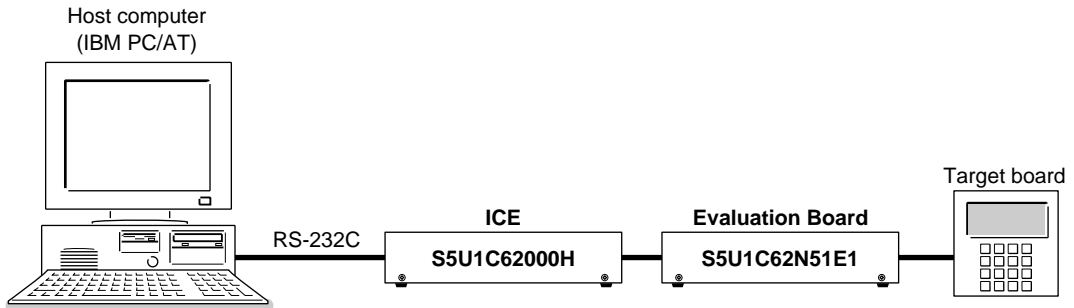


Fig. 5.1.1 Debugging system using ICE

☞ The functions of the ICE and commands are same as for the S1C62 Family. Refer to the "S1C62 Family Development Tool Reference Manual" for details.

## 5.2 ICS6002 Restrictions

Take the following precautions when using the ICS6002.

### ■ ROM Area

The ROM area is limited to a maximum address of 3FFH. Assigning data above the 3FFH address causes an error.

### ■ RAM Area

The RAM area is limited to a maximum address of 0FEH. However, as the following addresses are in the unused area, designation of this area with the ICE commands produces an error.

Unused area: 050H to 08FH, 0B0H to 0DFH, 0E1H, 0E2H, 0E9H, 0EAH, 0F2H

Memory 090H to 0AFH is display memory; 0E0H to 0FEH is I/O memory.  
(Refer to the "S1C60N02 Technical Manual" for details.)

### ■ Undefined Code

The instructions below are not specified for the S1C60N02 and so cannot be used.

SLP					
PUSH	XP	POP	XP	LD	XP,r
PUSH	YP	POP	YP	LD	YP,r
				LD	r,XP
				LD	r,YP

### ■ OPTLD Command

In the ICS6002, OPTLD command cannot be used.



## ■ Command list

Item No.	Function	Command Format	Outline of Operation
1	Assemble	#A,a [ ]	Assemble command mnemonic code and store at address "a"
2	Disassemble	#L,a1,a2 [ ]	Contents of addresses a1 to a2 are disassembled and displayed
3	Dump	#DP,a1,a2 [ ]	Contents of program area a1 to a2 are displayed
		#DD,a1,a2 [ ]	Content of data area a1 to a2 are displayed
4	Fill	#FP,a1,a2,d [ ]	Data d is set in addresses a1 to a2 (program area)
		#FD,a1,a2,d [ ]	Data d is set in addresses a1 to a2 (data area)
5	Set Run Mode	#G,a [ ]	Program is executed from the "a" address
		#TIM [ ]	Execution time and step counter selection
		#OTF [ ]	On-the-fly display selection
6	Trace	#T,a,n [ ]	Executes program while displaying results of step instruction from "a" address
		#U,a,n [ ]	Displays only the final step of #T,a,n
7	Break	#BA,a [ ]	Sets Break at program address "a"
		#BAR,a [ ]	Breakpoint is canceled
		#BD [ ]	Break condition is set for data RAM
		#BDR [ ]	Breakpoint is canceled
		#BR [ ]	Break condition is set for evaluation board CPU internal registers
		#BRR [ ]	Breakpoint is canceled
		#BM [ ]	Combined break conditions set for program data RAM address and registers
		#BMR [ ]	Cancel combined break conditions for program data ROM address and registers
		#BRES [ ]	All break conditions canceled
		#BC [ ]	Break condition displayed
		#BE [ ]	Enter break enable mode
		#BSYN [ ]	Enter break disable mode
8	Move	#MP,a1,a2,a3 [ ]	Contents of program area addresses a1 to a2 are moved to addresses a3 and after
		#MD,a1,a2,a3 [ ]	Contents of data area addresses a1 to a2 are moved to addresses a3 and after
9	Data Set	#SP,a [ ]	Data from program area address "a" are written to memory
		#SD,a [ ]	Data from data area address "a" are written to memory
10	Change CPU Internal Registers	#DR [ ]	Display evaluation board CPU internal registers
		#SR [ ]	Set evaluation board CPU internal registers
		#I [ ]	Reset evaluation board CPU
		#DXY [ ]	Display X, Y, MX and MY
		#SXY [ ]	Set data for X and Y display and MX, MY

Item No.	Function	Command Format	Outline of Operation
11	History	#H,p1,p2 <input type="checkbox"/>	Display history data for pointer 1 and pointer 2
		#HB <input type="checkbox"/>	Display upstream history data
		#HG <input type="checkbox"/>	Display 21 line history data
		#HP <input type="checkbox"/>	Display history pointer
		#HPS,a <input type="checkbox"/>	Set history pointer
		#HC,S/C/E <input type="checkbox"/>	Sets up the history information acquisition before (S), before/after (C) and after (E)
		#HA,a1,a2 <input type="checkbox"/>	Sets up the history information acquisition from program area a1 to a2
		#HAR,a1,a2 <input type="checkbox"/>	Sets up the prohibition of the history information acquisition from program area a1 to a2
		#HAD <input type="checkbox"/>	Indicates history acquisition program area
		#HS,a <input type="checkbox"/>	Retrieves and indicates the history information which executed a program address "a"
		#HSW,a <input type="checkbox"/>	Retrieves and indicates the history information which wrote or
#HSR,a <input type="checkbox"/>	read the data area address "a"		
12	File	#RF,file <input type="checkbox"/>	Move program file to memory
		#RFD,file <input type="checkbox"/>	Move data file to memory
		#VF,file <input type="checkbox"/>	Compare program file and contents of memory
		#VFD,file <input type="checkbox"/>	Compare data file and contents of memory
		#WF,file <input type="checkbox"/>	Save contents of memory to program file
		#WFD,file <input type="checkbox"/>	Save contents of memory to data file
		#CL,file <input type="checkbox"/>	Load ICE set condition from file
13	Coverage	#CVD <input type="checkbox"/>	Indicates coverage information
		#CVR <input type="checkbox"/>	Clears coverage information
14	ROM Access	#RP <input type="checkbox"/>	Move contents of ROM to program memory
		#VP <input type="checkbox"/>	Compare contents of ROM with contents of program memory
		#ROM <input type="checkbox"/>	Set ROM type
15	Terminate ICE	#Q <input type="checkbox"/>	Terminate ICE and return to operating system control
16	Command Display	#HELP <input type="checkbox"/>	Display ICE instruction
17	Self Diagnosis	#CHK <input type="checkbox"/>	Report results of ICE self diagnostic test

means press the RETURN key.

# 6 MASK DATA CHECKER MDC6002

## 6.1 MDC6002 Outline

The Mask Data Checker MDC6002 is a software tool which checks the program data (C002XXXH.HEX and C002XXXL.HEX) and option data (C002XXXF.DOC and C002XXXS.DOC) created by the user and creates the data file (C6002XXX.PAn) for generating mask patterns. The user must send the file generated through this software tool to Seiko Epson.

Moreover, MDC6002 has the capability to restore the generated data file (C6002XXX.PAn) to the original file format.

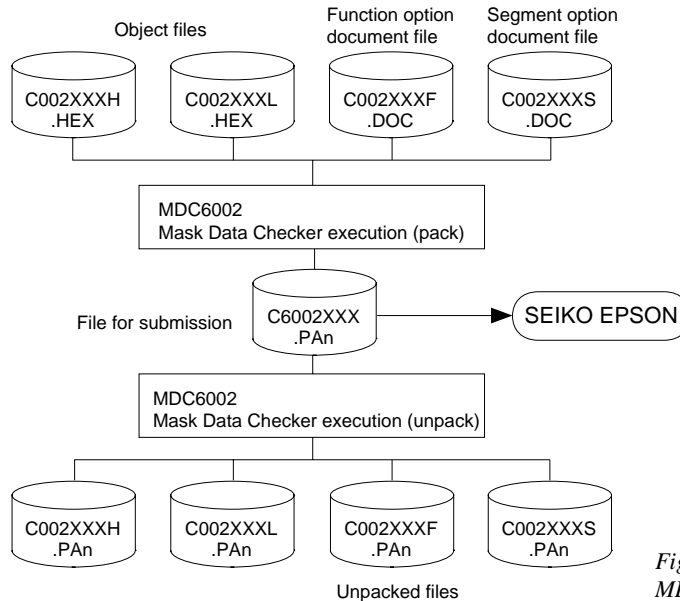


Fig. 6.1.1  
MDC6002 execution flow

☞ The operating method is same as for the S1C62 Family. Refer to the "S1C62 Family Development Tool Reference Manual" for details.

## 6.2 MDC6002 Quick Reference

### ■ Starting command and input/output files

**Execution file:** MDC6002.EXE

**Starting command:** **MDC6002**

indicates the Return key.

<b>Input file:</b>	C002XXXL.HEX (Object file, low-order)	] When packing
	C002XXXH.HEX (Object file, high-order)	
	C002XXXF.DOC (Function option document file)	
	C002XXXS.DOC (Segment option document file)	
	C6002XXX.PAn (Packed file)	
<b>Output file:</b>	C6002XXX.PAn (Packed file)	When packing
	C002XXXL.PAn (Object file, low-order)	] When unpacking
	C002XXXH.PAn (Object file, high-order)	
	C002XXXF.PAn (Function option document file)	
	C002XXXS.PAn (Segment option document file)	

■ Display examples

```

*** EOC6002 PACK / UNPACK PROGRAM Ver 2.00 ***

EEEEEEEEEE PFFFFFFP SSSSSSS OOOOOOOO NNN NNN
EEEEEEEEEE PFFFFFFP SSS SSS OOO OOO NNNN NNN
EEE PFP PFP SSS SSS OOO OOO NNNNN NNN
EEE PFP PFP SSS SSS OOO OOO NNNNN NNN
EEEEEEEEEE PFFFFFFP SSSSSSS OOO OOO NNN NNN NNN
EEEEEEEEEE PFFFFFFP SSSSSSS OOO OOO NNN NNNNN
EEE PFP SSS SSS OOO OOO NNN NNNNN
EEE PFP SSS SSS OOO OOO NNN NNNNN
EEEEEEEEEE PFP SSS SSS OOO OOO NNN NNN
EEEEEEEEEE PFP SSSSSSS OOOOOOOO NNN NN
    
```

(C) COPYRIGHT 1991 SEIKO EPSON CORP.

--- OPERATION MENU ---

1. PACK  
2. UNPACK

PLEASE SELECT NO.?

```

--- OPERATION MENU ---
1. PACK
2. UNPACK
PLEASE SELECT NO.? 1
C002XXXH.HEX -----+
C002XXXL.HEX -----+
C002XXXF.DOC -----+----- C002XXX.PAn (PACK FILE)
C002XXS.DOC -----+
PLEASE INPUT PACK FILE NAME (C6002XXX.PAn) ? C60020A0.PA0
C0020A0H.HEX -----+
C0020A0L.HEX -----+
C0020A0F.DOC -----+----- C0020A0.PA0
C0020A0S.DOC -----+
    
```

**Start-up message**

When MDC6002 is started, the start-up message and operation menu are displayed. Here, the user is prompted to select operation options.

**Packing of data**

- (1) Select "1.PACK" in the operation menu.
- (2) Enter the file name.

After submitting the data to Seiko Epson and there is a need to re-submit the data, increase the numeric value of "n" by one when the input is made. (Example: When re-submitting data after "C6002XXX.PA0" has been submitted, the pack file name should be entered as "C6002XXX.PA1".)

With this, the mask file (C6002XXX.PAn) is generated, and the MDC6002 program will be terminated. Submit this file to Seiko Epson.

*Note Don't use the data generated with the -N option of the Cross Assembler (ASM6002) as program data. If the program data generated with the -N option of the Cross Assembler is packed, undefined program area is filled with FFH code. In this case, following message is displayed.*

```

WARNING: FILLED <file_name> FILE WITH FFH.
    
```

```

--- OPERATION MENU ---
1. PACK
2. UNPACK
PLEASE SELECT NO.? 2
PLEASE INPUT PACKED FILE NAME (C6002XXX.PAn) ? C60020A0.PA0
C60020A0.PA0 -----+----- C0020A0H.PA0
|-----+----- C0020A0L.PA0
|-----+----- C0020A0F.PA0
|-----+----- C0020A0S.PA0
    
```

**Unpacking of data**

- (1) Select "2.UNPACK" in the operation menu.
- (2) Enter the packed file name.

With this, the mask data file (C6002XXX.PAn) is restored to the original file format, and the MDC6002 program will be terminated.

Since the extension of the file name remains as "PAn", it must be renamed back to its original form ("HEX" and "DOC") in order to re-debug or modify the restored file.

## ■ Error messages

### Program data error

Error Message	Explanation
1. HEX DATA ERROR : NOT COLON.	There is no colon.
2. HEX DATA ERROR : DATA LENGTH. (NOT 00-20h)	The data length of 1 line is not in the 00-20H range.
3. HEX DATA ERROR : ADDRESS.	The address is beyond the valid range of the program ROM.
4. HEX DATA ERROR : RECORD TYPE. (NOT 00)	The record type of 1 line is not 00.
5. HEX DATA ERROR : DATA. (NOT 00-FFh)	The data is not in the range between 00H and 0FFH.
6. HEX DATA ERROR : TOO MANY DATA IN ONE LINE.	There are too many data in 1 line.
7. HEX DATA ERROR : CHECK SUM.	The checksum is not correct.
8. HEX DATA ERROR : END MARK.	The end mark is not : 0000001FF.
9. HEX DATA ERROR : DUPLICATE.	There is duplicate definition of data in the same address.

### Function option data error

Error Message	Explanation
1. OPTION DATA ERROR : START MARK.	The start mark is not "\OPTION". (during unpacking) *
2. OPTION DATA ERROR : OPTION NUMBER.	The option number is not correct.
3. OPTION DATA ERROR : SELECT NUMBER.	The option selection number is not correct.
4. OPTION DATA ERROR : END MARK.	The end mark is not "\\END" (packing) or "\END" (unpacking).*

### Segment option data error

Error Message	Explanation
1. SEGMENT DATA ERROR : START MARK.	The start mark is not "\SEGMENT". (during unpacking) *
2. SEGMENT DATA ERROR : DATA.	The segment data is not correct.
3. SEGMENT DATA ERROR : SEGMENT NUMBER.	The SEG No. is not correct.
4. SEGMENT DATA ERROR : SPEC.	The output specification of the SEG terminal is not correct.
5. SEGMENT DATA ERROR : END MARK.	The end mark is not "\\END" (packing) or "\END" (unpacking).*

### File error

Error Message	Explanation
1. <File_name> FILE IS NOT FOUND.	The file is not found or the file number set in CONFIG.SYS is less than 10.
2. PACK FILE NAME (File_name) ERROR.	The packed input format for the file name is wrong.
3. PACKED FILE NAME (File_name) ERROR.	The unpacked input format for the file name is wrong.

### System error

Error Message	Explanation
1. DIRECTORY FULL.	The directory is full.
2. DISK WRITE ERROR.	Writing on the disk is failed.

\* \ sometimes appears as ¥, depending on the personal computer being used.

# APPENDIX A. S1C60N02 INSTRUCTION SET

Classification	Mnemonic	Operand	Operation Code								Flag			Clock	Operation					
			B	A	9	8	7	6	5	4	3	2	1			0	I	D	Z	C
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	l	0	0	0	1	l7	l6	l5	l4	l3	l2	l1	l0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← l3~l0, M(X+1) ← l7~l4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r*	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r*	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP*	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP*	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
		ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0	↑↓	↑↓			7
	XL, i		1	0	1	0	0	0	0	1	i3	i2	i1	i0	↑↓	↑↓			7	XL ← XL+i3~i0+C
	YH, i		1	0	1	0	0	0	1	0	i3	i2	i1	i0	↑↓	↑↓			7	YH ← YH+i3~i0+C
YL, i	1		0	1	0	0	0	1	1	i3	i2	i1	i0	↑↓	↑↓			7	YL ← YL+i3~i0+C	

\*: " mean "not in S1C60N02 Series".

Classification	Mnemonic	Operand	Operation Code						Flag			Clock	Operation							
			B	A	9	8	7	6	5	4	3			2	1	0	I	D	Z	C
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0	↑	↓			7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0	↑	↓			7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0	↑	↓			7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0	↑	↓			7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r ← i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r ← q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A ← M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B ← M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0) ← A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0) ← B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X) ← i3~i0, X ← X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r ← q, X ← X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y) ← i3~i0, Y ← Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r ← q, Y ← Y+1
LBPX	MX, l	1	0	0	1	17	16	15	14	13	12	11	10					5	M(X) ← 13~10, M(X+1) ← 17~14, X ← X+2	
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F ← F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F ← F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1			↑		7	C ← 1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0			↓		7	C ← 0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z ← 1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z ← 0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0			↑		7	D ← 1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1			↓		7	D ← 0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0			↑		7	I ← 1 (Enables Interrupt)
DI		1	1	1	1	0	1	0	1	0	1	1	1			↓		7	I ← 0 (Disables Interrupt)	
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP ← SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP ← SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP ← SP-1, M(SP) ← r
		XP *	1	1	1	1	1	1	0	0	0	1	0	0					5	SP ← SP-1, M(SP) ← XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP ← SP-1, M(SP) ← XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP ← SP-1, M(SP) ← XL
		YP *	1	1	1	1	1	1	0	0	0	1	1	1					5	SP ← SP-1, M(SP) ← YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP ← SP-1, M(SP) ← YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP ← SP-1, M(SP) ← YL
	F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP ← SP-1, M(SP) ← F	
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r ← M(SP), SP ← SP+1
		XP *	1	1	1	1	1	1	0	1	0	1	0	0					5	XP ← M(SP), SP ← SP+1
XH		1	1	1	1	1	1	0	1	0	1	0	1					5	XH ← M(SP), SP ← SP+1	
XL		1	1	1	1	1	1	0	1	0	1	1	0					5	XL ← M(SP), SP ← SP+1	
YP *		1	1	1	1	1	1	0	1	0	1	1	1					5	YP ← M(SP), SP ← SP+1	

\*" mean "not in S1C60N02 Series".

APPENDIX A. S1C60N02 INSTRUCTION SET

Classification	Mnemonic	Operand	Operation Code								Flag			Clock	Operation					
			B	A	9	8	7	6	5	4	3	2	1			0	I	D	Z	C
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH ← M(SP), SP ← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL ← M(SP), SP ← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↑	↓	↑	↓	5	F ← M(SP), SP ← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH ← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r ← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r ← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↓	↓	↓	7	r ← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↓	↓	↓	7	r ← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↓	↓	↓	7	r ← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↓	↓	↓	7	r ← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↓	↓	↓	7	r ← r-q
		r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↓	↓	↓	7	r ← r-i3~i0-C
	SBC	r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↓	↓	↓	7	r ← r-q-C
		r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↓			7	r ← r∧i3~i0
	AND	r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↓			7	r ← r∧q
		r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↓			7	r ← r∨i3~i0
	OR	r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↓			7	r ← r∨q
		r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↓			7	r ← r∨i3~i0
	XOR	r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↓			7	r ← r∨q
		r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↓			7	r ← r∨i3~i0
	CP	r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↓	↓		7	r-q
		r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↓			7	r∧i3~i0
	FAN	r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↓			7	r∧q
		r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↓	↓		7	d3 ← d2, d2 ← d1, d1 ← d0, d0 ← C, C ← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↓	↓		5	d3 ← C, d2 ← d3, d1 ← d2, d0 ← d1, C ← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↓	↓		7	M(n3~n0) ← M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↓	↓		7	M(n3~n0) ← M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↓	↓	↓	7	M(X) ← M(X)+r+C, X ← X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↓	↓	↓	7	M(Y) ← M(Y)+r+C, Y ← Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↓	↓	↓	7	M(X) ← M(X)-r-C, X ← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↓	↓	↓	7	M(Y) ← M(Y)-r-C, Y ← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↓			7	r ← r̄

Abbreviations used in the explanations have the following meanings.

**Symbols associated with registers and memory**

<b>A</b>	A register
<b>B</b>	B register
<b>X</b>	XHL register (low order eight bits of index register IX)
<b>Y</b>	YHL register (low order eight bits of index register IY)
<b>XH</b>	XH register (high order four bits of XHL register)
<b>XL</b>	XL register (low order four bits of XHL register)
<b>YH</b>	YH register (high order four bits of YHL register)
<b>YL</b>	YL register (low order four bits of YHL register)
<b>XP</b>	XP register (high order four bits of index register IX)
<b>YP</b>	YP register (high order four bits of index register IY)
<b>SP</b>	Stack pointer SP
<b>SPH</b>	High-order four bits of stack pointer SP
<b>SPL</b>	Low-order four bits of stack pointer SP
<b>MX, M(X)</b>	Data memory whose address is specified with index register IX
<b>MY, M(Y)</b>	Data memory whose address is specified with index register IY
<b>Mn, M(n)</b>	Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
<b>M(SP)</b>	Data memory whose address is specified with stack pointer SP
<b>r, q</b>	Two-bit register code r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Register specified
r1	r0	q1	q0	
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

**Symbols associated with program counter**

<b>NBP</b>	New bank pointer
<b>NPP</b>	New page pointer
<b>PCB</b>	Program counter bank
<b>PCP</b>	Program counter page
<b>PCS</b>	Program counter step
<b>PCSH</b>	Four high order bits of PCS
<b>PCSL</b>	Four low order bits of PCS

**Symbols associated with flags**

<b>F</b>	Flag register (I, D, Z, C)
<b>C</b>	Carry flag
<b>Z</b>	Zero flag
<b>D</b>	Decimal flag
<b>I</b>	Interrupt flag
↓	Flag reset
↑	Flag set
↕	Flag set or reset

**Associated with immediate data**

<b>p</b>	Five-bit immediate data or label 00H–1FH
<b>s</b>	Eight-bit immediate data or label 00H–0FFH
<b>l</b>	Eight-bit immediate data 00H–0FFH
<b>i</b>	Four-bit immediate data 00H–0FH

**Associated with arithmetic and other operations**

+	Add
-	Subtract
∧	Logical AND
∨	Logical OR
⊕	Exclusive-OR
★	Add-subtract instruction for decimal operation when the D flag is set

# APPENDIX B. S1C60N02 RAM MAP

PROGRAM NAME:																			
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	0	NAME MSB																	
		LSB																	
1	NAME MSB																		
		LSB																	
2	NAME MSB																		
		LSB																	
3	NAME MSB																		
		LSB																	
4	NAME MSB																		
		LSB																	
9	NAME MSB																		
		LSB																	
A	NAME MSB																		
		LSB																	
E	NAME MSB	K03				TM3	TC3	TC7	TC11	TC15	EIK03								
		K02				TM2	TC2	TC6	TC10	TC14	EIK02								
		K01				TM1	TC1	TC5	TC9	TC13	EIK01			EIT2					IT2
		K00				TM0	TC0	TC4	TC8	TC12	EIK00			EIT8					IT8
														EIT32	EIAD	IK0			IT32
F	NAME MSB					R03	P03	C3	C7	C11	C15		HLMOD	CSDC		XBZR			
						R02	P02	C2	C6	C10	C14								
						R01	P01	C1	C5	C9	C13								
						R00	P00	C0	C4	C8	C12	TMRST			IOC	XFOUT0	ADCLK		
		LSB	IAD	ADRUN															

# APPENDIX C. S1C60N02 I/O MEMORY MAP

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
0E0H	K03	K02	K01	K00	K03	-	High	Low	Input port data K03
					K02	-	High	Low	Input port data K02
	R				K01	-	High	Low	Input port data K01
					K00	-	High	Low	Input port data K00
0E3H	TM3	TM2	TM1	TM0	TM3	-	High	Low	Clock timer data 2 Hz
					TM2	-	High	Low	Clock timer data 4 Hz
	R				TM1	-	High	Low	Clock timer data 8 Hz
					TM0	-	High	Low	Clock timer data 16 Hz
0E4H	TC3	TC2	TC1	TC0	TC3	-	1	0	Up/down counter data TC3
					TC2	-	1	0	Up/down counter data TC2
	R/W				TC1	-	1	0	Up/down counter data TC1
					TC0	-	1	0	Up/down counter data TC0 (LSB)
0E5H	TC7	TC6	TC5	TC4	TC7	-	1	0	Up/down counter data TC7
					TC6	-	1	0	Up/down counter data TC6
	R/W				TC5	-	1	0	Up/down counter data TC5
					TC4	-	1	0	Up/down counter data TC4
0E6H	TC11	TC10	TC9	TC8	TC11	-	1	0	Up/down counter data TC11
					TC10	-	1	0	Up/down counter data TC10
	R/W				TC9	-	1	0	Up/down counter data TC9
					TC8	-	1	0	Up/down counter data TC8
0E7H	TC15	TC14	TC13	TC12	TC15	-	1	0	Up/down counter data TC15 (MSB)
					TC14	-	1	0	Up/down counter data TC14
	R/W				TC13	-	1	0	Up/down counter data TC13
					TC12	-	1	0	Up/down counter data TC12
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register K03
					EIK02	0	Enable	Mask	Interrupt mask register K02
	R/W				EIK01	0	Enable	Mask	Interrupt mask register K01
					EIK00	0	Enable	Mask	Interrupt mask register K00
0EBH	0	EIT2	EIT8	EIT32	0				
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer) 2 Hz
	R	R/W			EIT8	0	Enable	Mask	Interrupt mask register (clock timer) 8 Hz
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer) 32 Hz
0ECH	0	0	0	EIAD	0				
	R			R/W	0				
					EIAD	0	Enable	Mask	Interrupt mask register (A/D)
0EDH	0	0	0	IK0	0				
	R				0				
					IK0	0	Yes	No	Interrupt factor flag (K00-K03)
0EFH	0	IT2	IT8	IT32	0				
					IT2	0	Yes	No	Interrupt factor flag (clock timer) 2 Hz
	R				IT8	0	Yes	No	Interrupt factor flag (clock timer) 8 Hz
					IT32	0	Yes	No	Interrupt factor flag (clock timer) 32 Hz

APPENDIX C. S1C60N02 I/O MEMORY MAP

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
0F0H	0	0	0	IAD	0 0 0				Interrupt factor flag (A/D)
	R				IAD	0	Yes	No	
0F1H	0	0	0	ADRUN	0 0 0				A/D conversion Start/Stop
	R			R/W	ADRUN	0	Start	Stop	
0F3H	R03	R02	R01	R00	R03	0	High	Low	Output port data R03
			BUZZER	FOUT	R02	0	High	Low	Output port data R02
	R/W				R01	0	High	Low	Output port data R01
	R/W				BUZZER	0	On	Off	Buzzer On/Off control register
R/W				R00	0	High	Low	Output port data R00	
R/W				FOUT	0	On	Off	Frequency output control register	
0F4H	P03	P02	P01	P00	P03	–	High	Low	I/O port data P03
	R/W				P02	–	High	Low	I/O port data P02
	R/W				P01	–	High	Low	I/O port data P01
	R/W				P00	–	High	Low	I/O port data P00
0F5H	C3	C2	C1	C0	C3	–	1	0	Up-counter data C3
	R/W				C2	–	1	0	Up-counter data C2
	R/W				C1	–	1	0	Up-counter data C1
	R/W				C0	–	1	0	Up-counter data C0 (LSB)
0F6H	C7	C6	C5	C4	C7	–	1	0	Up-counter data C7
	R/W				C6	–	1	0	Up-counter data C6
	R/W				C5	–	1	0	Up-counter data C5
	R/W				C4	–	1	0	Up-counter data C4
0F7H	C11	C10	C9	C8	C11	–	1	0	Up-counter data C11
	R/W				C10	–	1	0	Up-counter data C10
	R/W				C9	–	1	0	Up-counter data C9
	R/W				C8	–	1	0	Up-counter data C8
0F8H	C15	C14	C13	C12	C15	–	1	0	Up-counter data C15 (MSB)
	R/W				C14	–	1	0	Up-counter data C14
	R/W				C13	–	1	0	Up-counter data C13
	R/W				C12	–	1	0	Up-counter data C12
0F9H	0	0	0	TMRST	0 0 0				Clock timer reset
	R			W	TMRST	Reset	Reset	–	
0FAH	HLMOD	0	0	0	HLMOD	0	Heavy	Normal	Heavy load protection mode register
	R/W	R			0 0				
0FBH	CSDC	0	0	0	CSDC	0	Static	Dynamic	LCD drive switch
	R/W	R			0 0				
0FCH	0	0	0	IOC	0 0 0				I/O port I/O control register
	R			R/W	IOC	0	Out	In	
0FDH	XBZR	0	XFOUT1	XFOUT0	XBZR	0	2 kHz	4 kHz	Buzzer frequency control
	R/W				XFOUT1	0			FOUT frequency control
	R/W				XFOUT0	0			FOUT frequency control
0FEH	0	0	0	ADCLK	0 0 0				A/D clock selection 65 kHz/32 kHz
	R			R/W	ADCLK	0	65 kHz	32 kHz	

# APPENDIX D. TROUBLESHOOTING

Tool	Problem	Remedy measures
ICE S5U1C62000H	Nothing appears on the screen, or nothing works, after activation.	Check the following and remedy if necessary: <ul style="list-style-type: none"> <li>• Is the RS-232C cable connected correctly?</li> <li>• Is the RS-232C driver installed?</li> <li>• Is MODE.COM on the disk?</li> <li>• Is the execution file correct? PC-DOS ICS6002W.EXE</li> <li>• Is the DOS version correct? PC-DOS Ver. 2.1 or later</li> <li>• Is the DIP switches that set the baud rate of the main ICE unit set correctly?</li> <li>• Is the fuse of the ICE cut off?</li> </ul>
	The ICE fuse cut immediately after activation.	Check the following and remedy if necessary: <ul style="list-style-type: none"> <li>• Are connectors F1 and F5 connected to the evaluation board correctly?</li> <li>• Is the target board power short-circuiting?</li> </ul>
	<ILLEGAL VERSION ICE6200> appears on the screen immediately after activation.	The wrong version of ICE is being used. Use the latest version.
	<ILLEGAL VERSION PARAMETER FILE> appears on the screen immediately after activation.	The wrong version of ICS6002P.PAR is being used. Use the latest version.
	Immediate values A (10) and B (11) cannot be entered correctly with the A command.	The A and B registers are reserved for the entry of A and B. Write 0A and 0B when entering A (10) and B (11). <i>Example:</i> LD A, B Data in the B register is loaded into the A register. LD B, 0A Immediate value A is loaded into the B register.
	<UNUSED AREA> is displayed by the SD command.	This message is output when the address following one in which data is written is unused. It does not indicate problem. Data is correctly set in areas other than the read-only area.
	You can not do a real-time run in break-trace mode.	Since the CPU stops temporarily when breaking conditions are met, executing in a real-time is not performed.
	Output from the evaluation board is impossible when data is written to the I/O memory for Buzzer and Fout output with the ICE command.	Output is possible only in the real-time run mode.
SOG6002	An R error occurs although the address is correctly set in the segment source file.	Check the following and remedy if necessary: <ul style="list-style-type: none"> <li>• Does the address symbol use capital letters?</li> <li>• Are the output ports set for every two terminals?</li> </ul>

APPENDIX D. TROUBLESHOOTING

Tool	Problem	Remedy measures
ASM6002	An R error occurs although the final page is passed.	The cross assembler is designed to output "R error" every time the page is changed. Use a pseudo-instruction to set the memory, such as ORG or PAGE, to change the page. See "Memory setting pseudo-instructions" in the cross assembler manual.
MDC6002	Activation is impossible.	Check the following and remedy if necessary: <ul style="list-style-type: none"> <li>• Is the number of files set at ten or more in OS environment file CONFIG.SYS?</li> </ul>
Evaluation board S5U1C62N51E1	The evaluation board does not work when it is used independently.	Check the following and remedy if necessary: <ul style="list-style-type: none"> <li>• Has the EPROM for F.HEX and S.HEX been replaced by the EPROM for the target?</li> <li>• Is the EPROM for F.HEX and S.HEX installed correctly?</li> <li>• Is the appropriate voltage being supplied? (5V DC, 3A, or more)</li> <li>• Are the program ROMs (H and L) installed correctly?</li> <li>• Is data written from address 4000H? (When the 27C256 is used as the program ROM)</li> <li>• Is the EN/DIS switch on the evaluation board set to EN?</li> </ul>
	Target segment does not light.	Check the following and remedy if necessary: <ul style="list-style-type: none"> <li>• Is an EPROM with an access time of 170 ns or less being used for S.HEX.</li> <li>• Has the VADJ VR inside the evaluation board top cover been turned to a lower setting?</li> </ul>

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### EPSON EUROPE ELECTRONICS GmbH

#### - HEADQUARTERS -

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80992 Munich, GERMANY  
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

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No. 1 Temasek Avenue, #36-00  
Millenia Tower, SINGAPORE 039192  
Phone: +65-337-7911 Fax: +65-334-2716

### SEIKO EPSON CORPORATION KOREA OFFICE

50F, KLI 63 Bldg., 60 Yoido-dong  
Youngdeungpo-Ku, Seoul, 150-763, KOREA  
Phone: 02-784-6027 Fax: 02-767-3677

### SEIKO EPSON CORPORATION

#### ELECTRONIC DEVICES MARKETING DIVISION

##### Electronic Device Marketing Department

##### IC Marketing & Engineering Group

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN  
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

##### ED International Marketing Department Europe & U.S.A.

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421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN  
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