

S1R72E11

Data Sheet

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Scope of Application

This document applies to “S1R72E11”, a SD/MMC host controller LSI.

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1. OVERVIEW

The S1R72E11 is a SD/MMC host controller LSI that can be connected to the 16-bit general-purpose memory bus on the main processor.

2. FEATURES

<<SD host function>>

- Compliant with SD specification Ver.2.0
- Transfer clock: Up to 50 MHz
- Supports SDHC cards
- Bus width: 4 bits/1 bit

<<MMC host function>>

- Compliant with MMC specification Ver. 4.2. (CE-ATA Ver. 1.1 compliant.)
- Transfer clock: Up to 50 MHz
- Supports high-capacity cards.
- Bus width: 8 bits/4 bits/1 bit

<<CPU interface (CPU-IF) function>>

- 16-bit general-purpose CPU bus interface
- DMA 1ch
- Supports little endian/big endian.

<<Others>>

- Clock: Supports external clock input or crystal oscillator. Up to 50 MHz.
- Power management: Includes the sleep function (oscillator circuit halt mode).
- Power supply voltage: 3.3 V+/- 0.3 V, single
- Package: TQFP13-64pin
- Guaranteed operating temperature: -40 °C to 85 °C

3. BLOCK DIAGRAM

3. BLOCK DIAGRAM

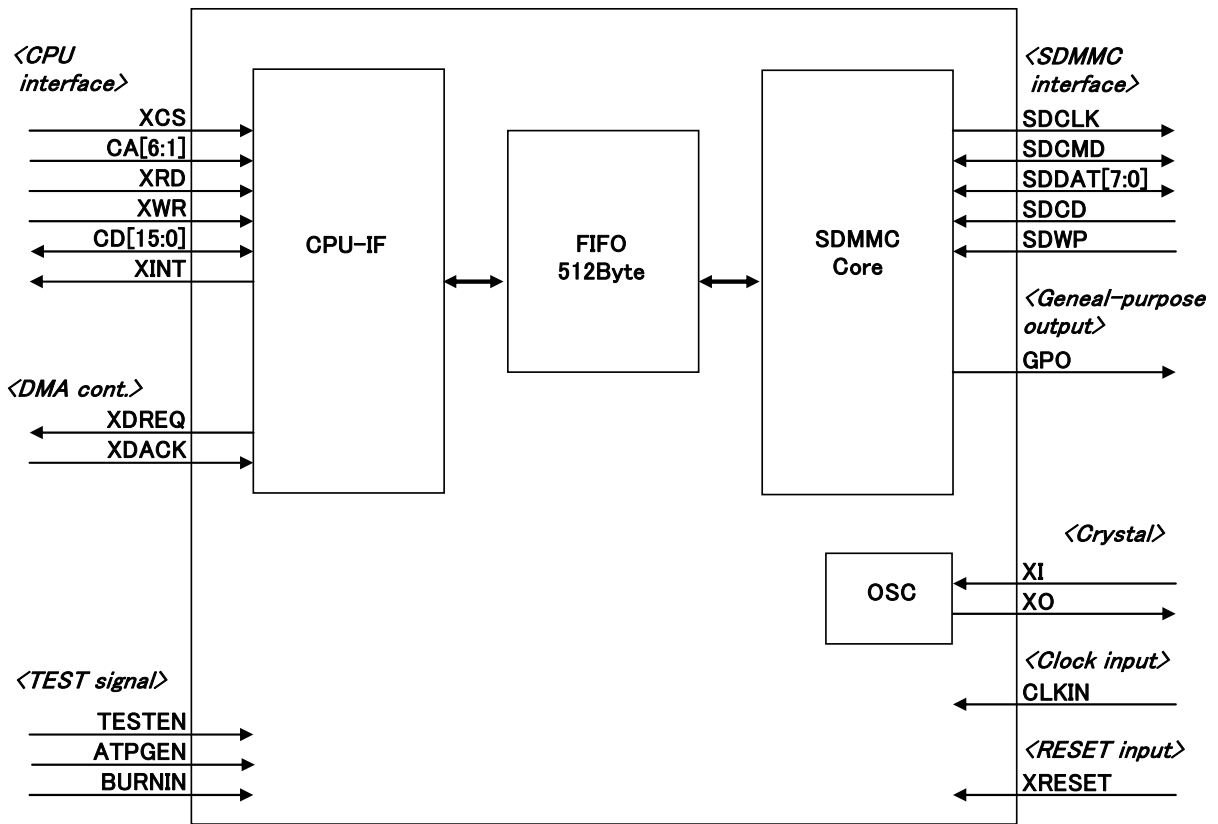


Figure 3.1 Overall Block Diagram

4. PIN ASSIGNMENT

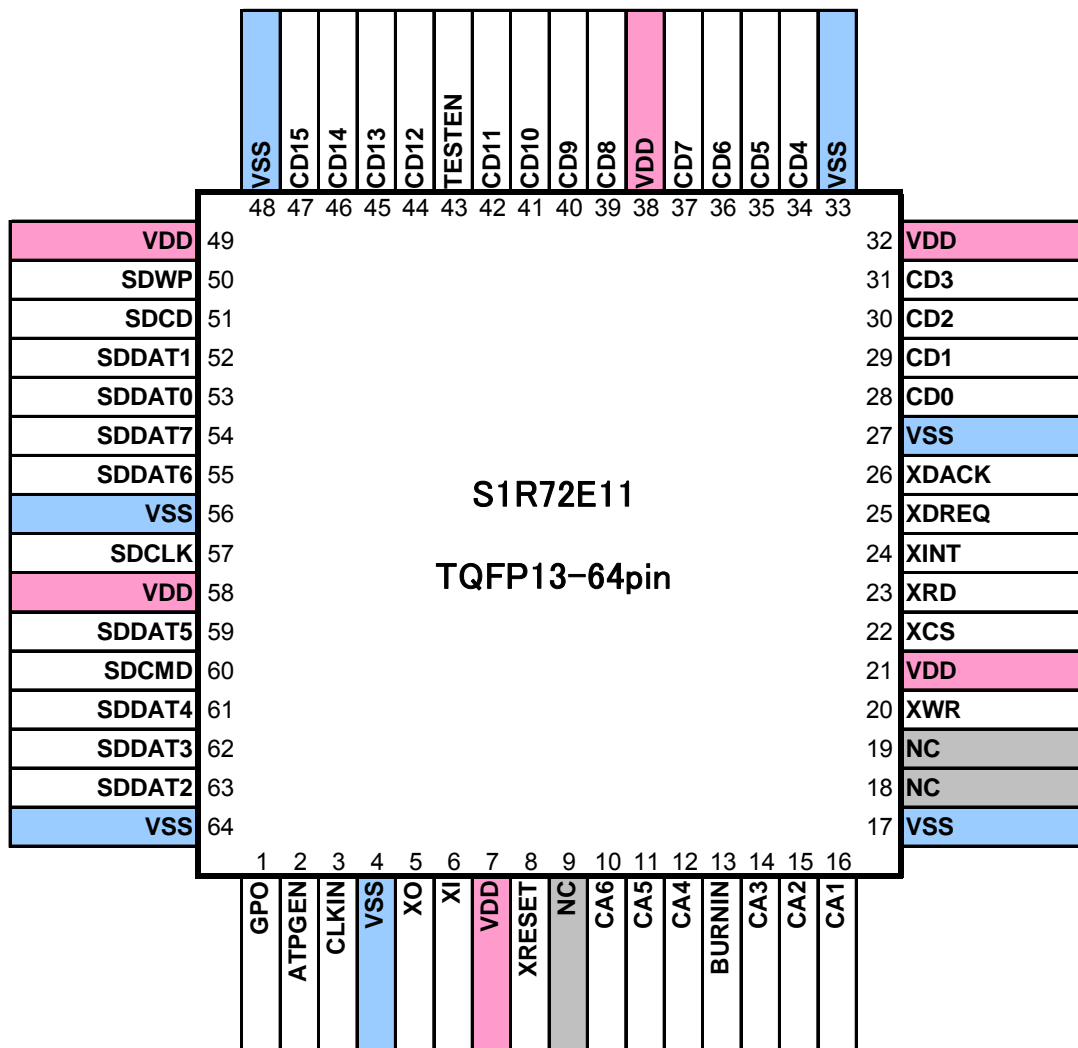


Figure 4.1 Pin Assignment

5. PIN DESCRIPTION

5. PIN DESCRIPTION

CPU-I/F					
QFP-Pin	Name	I/O	RESET	Pin Type	Pin Description
22	XCS	IN	—	(PU)	Chip select
10	CA6	IN	—	—	CPU bus address
11	CA5	IN	—	—	
12	CA4	IN	—	—	
14	CA3	IN	—	—	
15	CA2	IN	—	—	
16	CA1	IN	—	—	
23	XRD	IN	—	—	Read strobe
20	XWR	IN	—	—	Write strobe
47	CD15	BI	Hi-Z	2mA	CPU bus high data
46	CD14	BI	Hi-Z	2mA	
45	CD13	BI	Hi-Z	2mA	
44	CD12	BI	Hi-Z	2mA	
42	CD11	BI	Hi-Z	2mA	
41	CD10	BI	Hi-Z	2mA	
40	CD9	BI	Hi-Z	2mA	
39	CD8	BI	Hi-Z	2mA	
37	CD7	BI	Hi-Z	2mA	CPU bus low data
36	CD6	BI	Hi-Z	2mA	
35	CD5	BI	Hi-Z	2mA	
34	CD4	BI	Hi-Z	2mA	
31	CD3	BI	Hi-Z	2mA	
30	CD2	BI	Hi-Z	2mA	
29	CD1	BI	Hi-Z	2mA	
28	CD0	BI	Hi-Z	2mA	
24	XINT	OUT	High	2mA (Tri-State)	Interrupt output

PU: Pull Up

DMA control					
QFP-Pin	Name	I/O	RESET	Pin type	Pin Description
25	XDREQ	OUT	High	2mA	DMA request
26	XDACK	IN	—	—	DMA acknowledgment

When DMA is not used: XDREQ = Open. XDACK = fixed to High or Low

SDMMC-IF						
QFP-Pin	Name	I/O	RESET	Pin type	Pin Description	
57	SDCLK	OUT	Low	6mA	SD/MMC bus clock	
60	SDCMD	BI	Hi-Z	6mA	SD/MMC command line	
54	SDDAT7(GPIO3)	BI	Hi-Z	6mA	SD/MMC data bus	SD/MMC data bus
55	SDDAT6(GPIO2)	BI	Hi-Z	6mA		
59	SDDAT5(GPIO1)	BI	Hi-Z	6mA	SD/MMC data bus	
61	SDDAT4(GPIO0)	BI	Hi-Z	6mA		
62	SDDAT3	BI	Hi-Z	6mA		
63	SDDAT2	BI	Hi-Z	6mA		
52	SDDAT1	BI	Hi-Z	6mA		
53	SDDAT0	BI	Hi-Z	6mA		
51	SDCD	IN	—	—	SD/MMC card detect	
50	SDWP	IN	—	—	SD/MMC write protect	

When SDDAT[7:4] is not used: SDDAT[7:4] = fixed to High or Low

General-purpose output					
QFP-Pin	Name	I/O	RESET	Pin type	Pin Description
1	GPO	OUT	Low	6mA	General-purpose output port (LED control)

When general-purpose output is not used: GPO = Open.

Crystal oscillator (when CLKIN is not used)					
QFP-Pin	Name	I/O	RESET	Pin type	Pin Description
6	XI	IN	—	Analog	Input for built-in oscillation circuit
5	XO	OUT	—	Analog	Output for built-in oscillation circuit

When crystal oscillator is not used: XI pin = fixed to High or Low XO pin = Open.

Clock input (when crystal oscillator is not used)					
QFP-Pin	Name	I/O	RESET	Pin type	Pin Description
3	CLKIN	IN	—	—	External clock input

When the CLKIN pin is not used: CLKIN = fixed to High or Low.

Reset input					
QFP-Pin	Name	I/O	RESET	Pin type	Pin Description
8	XRESET	IN	—	Schmitt	Reset input

5. PIN DESCRIPTION

TEST signal

QFP-Pin	Name	I/O	RESET	Pin type	Pin Description
43	TESTEN	IN	(PD)	(PD)	Test pin (fixed to Low)
2	ATPGEN	IN	(PD)	(PD)	Test pin (fixed to Low)
13	BURNIN	IN	(PD)	(PD)	Test pin (fixed to Low)

PD: Pull Down

NC

QFP-Pin	Name	I/O	RESET	Pin type	Pin Description
9,18,19	NC	—	—	—	Unused pin

POWER

QFP-Pin	Name	I/O	Voltage	Pin Description
7,21,32,38,49,58	VDD	IN	3.3V	Power supply
4,17,27,33,48,56,64	VSS	IN	0V	GND

6. FUNCTIONAL DESCRIPTION

6.1 Reset

The LSI has the hard reset and the soft reset functions, using the external XRESET pin and the register setting respectively.

Upon power-on, start the LSI in the hard reset state using the XRESET pin, and release the hard reset after the power is stabilized.

For the procedure of initialization after the hard reset, see the Technical Manual.

6.2 Clock

The LSI includes an oscillator, and supports clock generation using an external oscillator.

The LSI also supports the external clock input from the CLKIN pin.

The following illustrates an example to connect the oscillation circuit. Rf, Rd, C1 and C2 on the oscillation circuit shown in the figure must be fitted together using an oscillator. For the circuit constants, consult with the oscillator manufacturer.

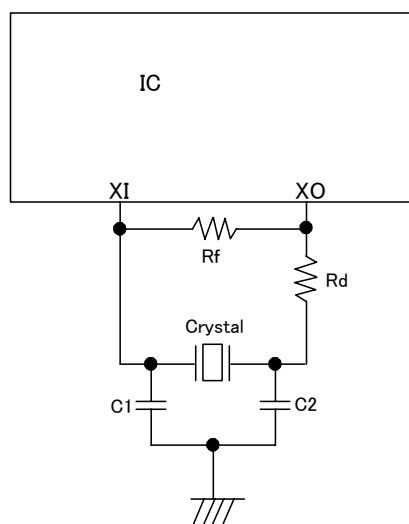


Figure 6.1 Example of Oscillation Circuit Connection

6.3 CPU-IF

The LSI can be connected to the 16-bit general purpose memory bus on the main processor. The following table provides truth values for each CPU interface mode.

Table 6.1 CPU Interface Truth Table

XCS	XRD	XWR	CD[15:0]
H	X	X	Hi-Z
L	L	H	Read
L	H	L	Write

6. FUNCTIONAL DESCRIPTION

6.4 Power Management

The LSI includes the power management function and has dual power management states, that is sleep and active.

All function blocks are operating in the active state.

In the sleep state, only the minimum circuits operate required for returning from the standby state, and only the asynchronous registers are accessible.

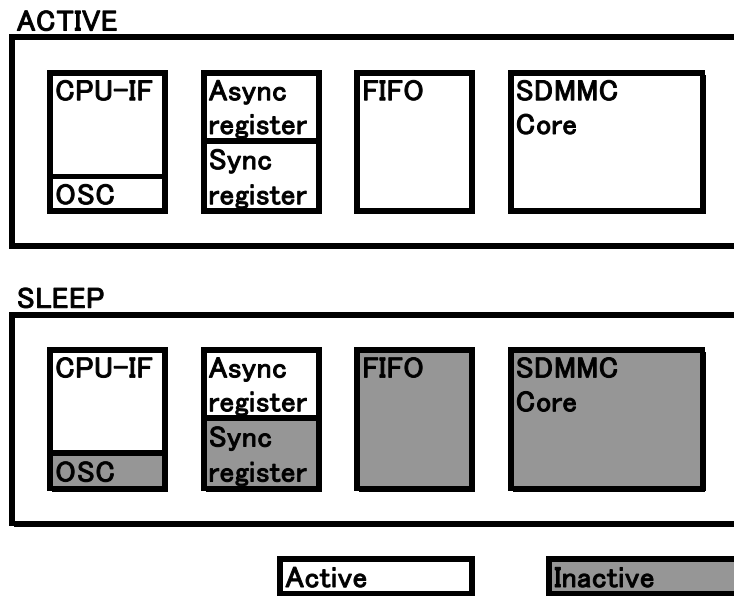


Figure 6.2 Power Management State

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

(V_{SS}=0V)

Item	Symbol	Rating	Unit
Power voltage	V _{DD}	V _{SS} - 0.3 to 4.0	V
Input voltage	V _I	V _{SS} - 0.3 to V _{DD} + 0.5	V
Output voltage	V _O	V _{SS} - 0.3 to V _{DD} + 0.5	V
Output current/pin	I _O	±30	mA
Storage temperature	T _{stg}	-65 to 150	°C

7.2 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power voltage	V _{DD}	3.0	3.3	3.6	V
Input voltage	V _I	-0.3	—	V _{DD}	V
Ambient temperature	T _a	-40	25	85 *1	°C

(Note) *1 This ambient temperature range represents a recommended one assuming T_j = -40 - 125 °C.

7. ELECTRICAL CHARACTERISTICS

7.3 DC Characteristics

7.3.1 Current Consumption

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply current: When read/write access to SD card in ACTIVE mode(*)						
Power current	IDD1	V _{DD} = 3.3V	—	45	—	mA
Static current						
Power current	IDDS	V _I = V _{DD} or V _{SS} V _{DD} = 3.6V	—	—	35	μA
Input leak						
Input leak current	IL	V _{DD} = 3.6V V _{IH} = V _{DD} V _{IL} = V _{SS}	-1	—	1	μA

* Average current in the recommended operating condition (Ta = 25 °C)

7.3.2 Input Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input characteristics Pin name: CA[6:1], XRD, XWR, CD[15:0], XDACK, SDCMD, SDDAT[7:0], SDCD, SDWP, CLKIN, TESTEN, ATPGEN, BURNIN						
High level input voltage	VIH1	V _{DD} = 3.6V	2.0	—	3.6-	V
Low level input voltage	VIL1	V _{DD} = 3.0V	-0.3	—	0.8	V
Input characteristics (Schmitt) Pin name: XRESET, XCS						
High level trigger voltage	VT1+	—	1.1	—	2.4	V
Low level trigger voltage	VT1-	—	0.6	—	1.8	V
Hysteresis voltage	ΔV1	—	0.1	—	—	V
Input characteristics Pin name: XCS						
Pull-up resistor	RPU2	V _I = V _{SS}	40	100	240	kΩ
Input characteristics Pin name: TSTEN						
Pull-down resistor	RPD1	V _I = V _{DD}	20	50	120	kΩ
Input characteristics Pin name: ATPGEN, BURNIN						
Pull-down resistor	RPD2	V _I = V _{DD}	40	100	240	kΩ

7. ELECTRICAL CHARACTERISTICS

7.3.3 Output Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output characteristics	Pin name: CD[15:0], XDREQ					
High level output voltage	VOH1	V _{DD} = 3.0V I _{OH} = -2.0mA	V _{DD} - 0.4	—	—	V
Low level output voltage	VOL1	V _{DD} = 3.0V I _{OL} = 2.0mA	—	—	0.4	V
Output characteristics	Pin name: SDCLK, SDCMD, SDDAT[7:0], GPO					
High level output voltage	VOH2	V _{DD} = 3.0V I _{OH} = -6.0mA	V _{DD} - 0.4	—	—	V
Low level output voltage	VOL2	V _{DD} = 3.0V I _{OL} = 6.0mA	—	—	0.4	V
Output characteristics	Pin name: XINT					
Off-state leak current	IOZ	V _{DD} = 3.6V V _{OH} = V _{DD} V _{OL} = V _{SS}	-1	—	1	μA

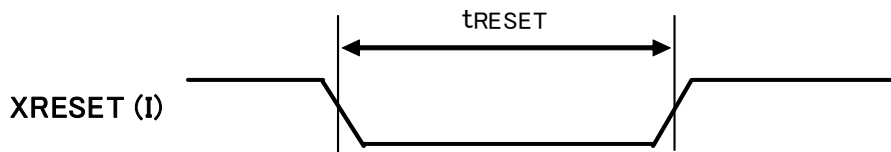
7.3.4 Output characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Pin capacity	Pin name: All input pins					
Input pin capacity	CI	f = 1MHz V _{DD} = V _{SS}	—	—	10	pF
Pin capacity	Pin name: All output pins					
Output pin capacity	CO	f = 1MHz V _{DD} = V _{SS}	—	—	10	pF
Pin capacity	Pin name: All I/O pins					
I/O pin capacity	CB	f = 1MHz V _{DD} = V _{SS}	—	—	10	pF

7. ELECTRICAL CHARACTERISTICS

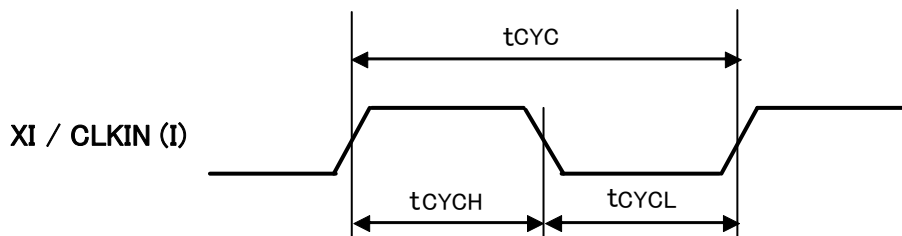
7.4 AC Characteristics

7.4.1 Reset Timing



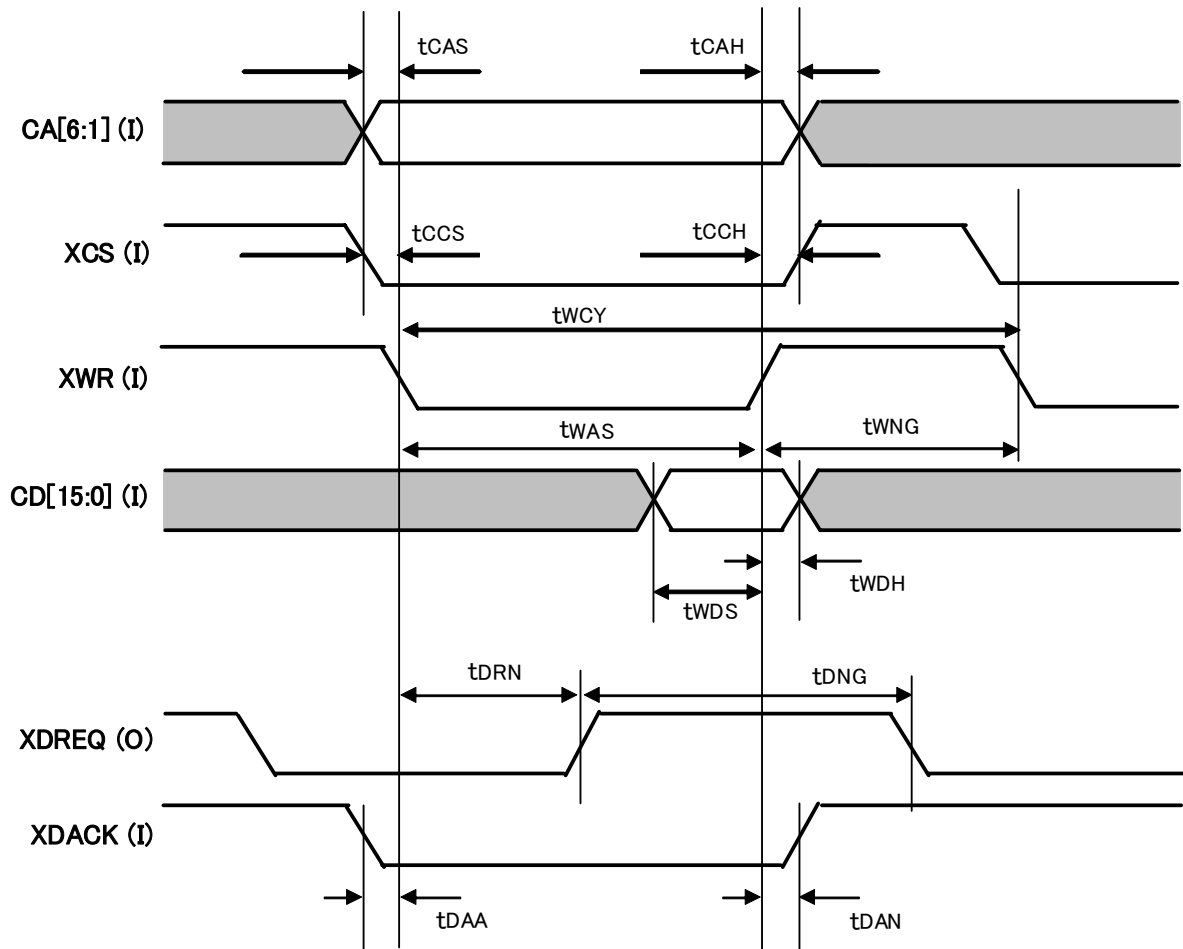
Symbol	Parameter	Min.	Typ.	Max.	Unit
tRESET	RESET pulse width	40	—	—	ns

7.4.2 Clock Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
tCYC	Clock cycle	—	—	50	MHz
tCYCH tCYCL	Clock High / Low width	9.0	—	—	ns

7.4.3 CPU/DMA Interface Write Access Timing



Conditions: $C_l = 30\text{pf}$

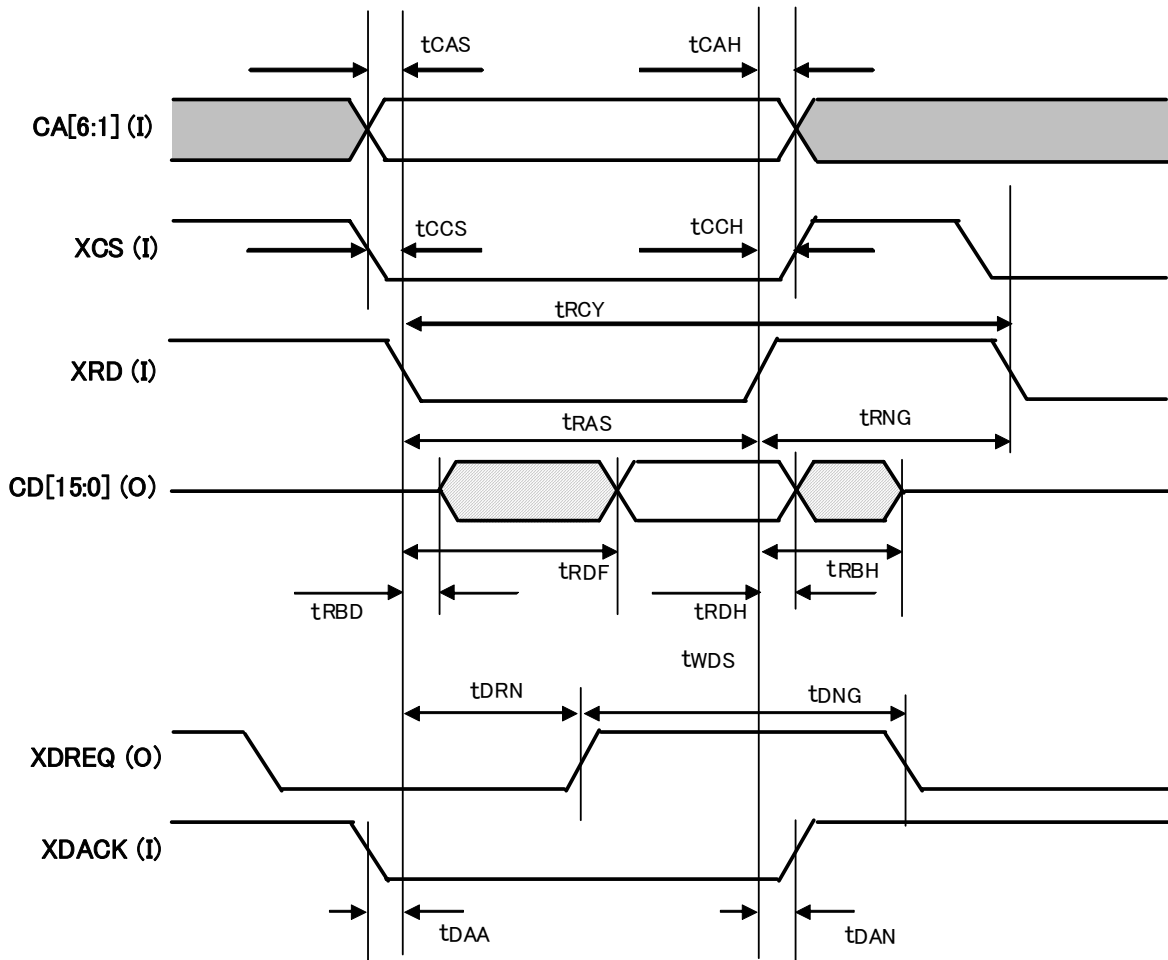
Symbol	Parameter	Min.	Typ.	Max.	Unit
tCAS	CA[6:1] setup time to negative edge of XWR	2	—	—	ns
tCAH	CA[6:1] hold time from positive edge of XWR	6	—	—	ns
tCCS	XCS setup time to negative edge of XWR	0	—	—	ns
tCCH	XCS hold time from positive edge of XWR	0	—	—	ns
tWCY	XWR access time	$(3 \times TC)+10$	—	—	ns
tWAS	XWR assert pulse width	$(2 \times TC)+10$	—	—	ns
tWNG	XWR negate pulse width	TC	—	—	ns
tWDS	CD[15:0] setup time to negative edge of XWR	10	—	—	ns
tWDH	CD[15:0] hold time from positive edge of XWR	8	—	—	ns
tDRN	XDREQ negate delay from negative edge of XWR	—	—	$(2 \times TC)+15$	ns
tDNG	XDREQ negate time from positive edge of XDREQ	$RN \times TC$	—	—	ns
tDAA	XDACK setup time to negative edge of XWR	0	—	—	ns
tDAN	XDACK hold time from positive edge of XWR	0	—	—	ns

TC = Input clock cycle (Example: 20 ns for 50 MHz clock input)

RN = 1 + the set value of the DMA_Config.NgtCnt[3:0] register

7. ELECTRICAL CHARACTERISTICS

7.4.4 CPU/DMA Interface Read Access Timing



Cl = 30pf

Symbol	Parameter	Min.	Typ.	Max.	Unit
tCAS	CA[6:1] setup time to negative edge of XRD	2	—	—	ns
tCAH	CA[6:1] hold time from positive edge of XRD	6	—	—	ns
tCCS	XCS setup time to negative edge of XRD	0	—	—	ns
tCCH	XCS hold time from positive edge of XRD	0	—	—	ns
tRCY	XRD access time	(3 x TC)+30	—	—	ns
tRAS	XRD assert pulse width	(2 x TC)+30	—	—	ns
tRNG	XRD negate pulse width	TC	—	—	ns
tRBD	CD[15:0] driven delay from negative edge of XRD	2	—	—	ns
tRDF	CD[15:0] Valid Data delay from negative edge of XRD	—	—	(2 x TC)+30	ns
tRDH	CD[15:0] hold time from positive edge of XRD	2	—	—	ns
tRBH	CD[15:0] release delay from positive edge of XRD	—	—	15	ns
tDRN	XDREQ negate delay from negative edge of XRD	—	—	(2 x TC)+15	ns
tDNG	XDREQ negate time from positive edge of XDREQ	RN x TC	—	—	ns
tDAA	XDACK setup time to negative edge of XRD	0	—	—	ns
tDAN	XDACK hold time from positive edge of XRD	0	—	—	ns

TC = Input clock cycle (Example: 20 ns for 50 MHz clock input)

RN = 1 + the set value of the DMA_Config.NgtCnt[3:0] register

7.4.5 SDMMC Interface Timing

Complies with the SD 2.0 standard.

See “SD Specifications Part1 Physical Layer Specification Version 2.00” specification.

8. CONNECTION EXAMPLES

8. CONNECTION EXAMPLES

8.1 An Example of CPU Interface Connection

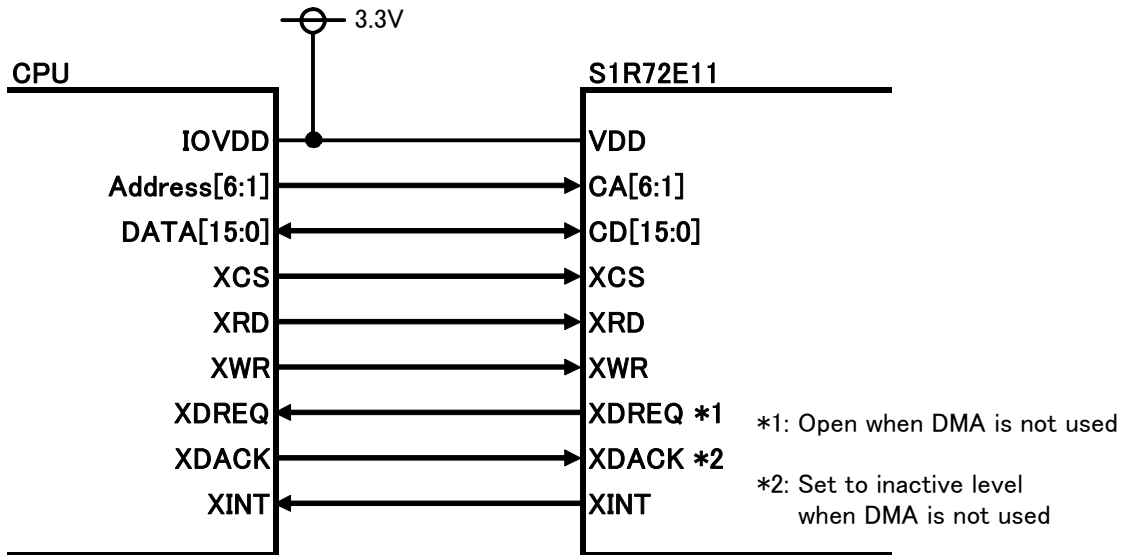


Figure 8.1 Example of CPU Interface Connection

9. MODEL NUMBER

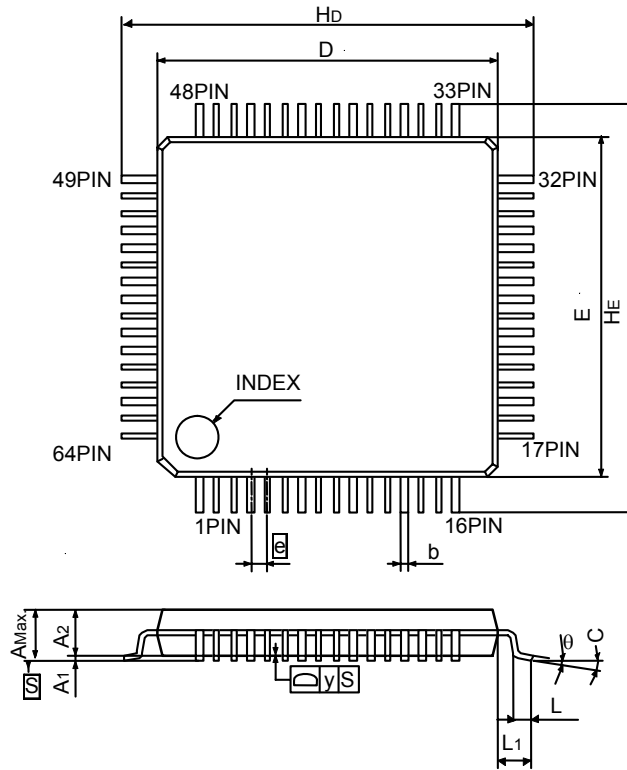
Table 9.1 Product model number

Model No.	Product type
S1R72E11F13E10****	TQFP13-64 package

10. EXTERNAL DIMENSIONS

10. EXTERNAL DIMENSIONS

10.1 TQFP13-64pin



Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
E	—	10	—
D	—	10	—
A_{max}	—	—	1.2
A_1	—	0.1	—
A_2	—	1	—
e	—	0.5	—
b	0.17	—	0.27
c	0.09	—	0.2
θ	0°	—	10°
L	0.3	—	0.75
L_1	—	1	—
H_E	—	12	—
H_D	—	12	—
y	—	—	0.08

1 = 1mm

REVISION HISTORY

	Rev.	Page	Type	Description
09/3/31	1.00	Full page	New	Newly established.
09/7/17	1.10	-	Amended	Amended NOTICE.

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