# Performance Requirements for Reference Clocks for 5G Communications

OUT-20-5536 Rev.2

## Overview

The proliferation of data demand in recent years has given rise to the deployment of high-speed 5th-generation communication systems (5G), for mobile communications, the Internet of Things (IoT), and Advanced Driver Assistance Systems (ADAS).

To keep up with the increased demand for data, communications capacity must continue to increase by adopting faster data rates and allocating more bandwidth. Faster data rates and higher bandwidths require precision clocks and pose stringent requirements on the permissible noise levels.

Here, we explain the 5G communication system situation, the performance required for reference clocks, and Epson's efforts in these areas.

## 5G communication systems and the market

5G communication systems consist of 5G base stations (macro-cell base stations and small cell base stations) that communicate wirelessly with each device, and mobile backhauls that connect the base stations to the core and metro networks, which in turn connect the base stations to the data centers. With the migration from LTE to 5G, networks must support massively increased throughput, higher numbers of connected devices, and ultra-reliable low latency communications.

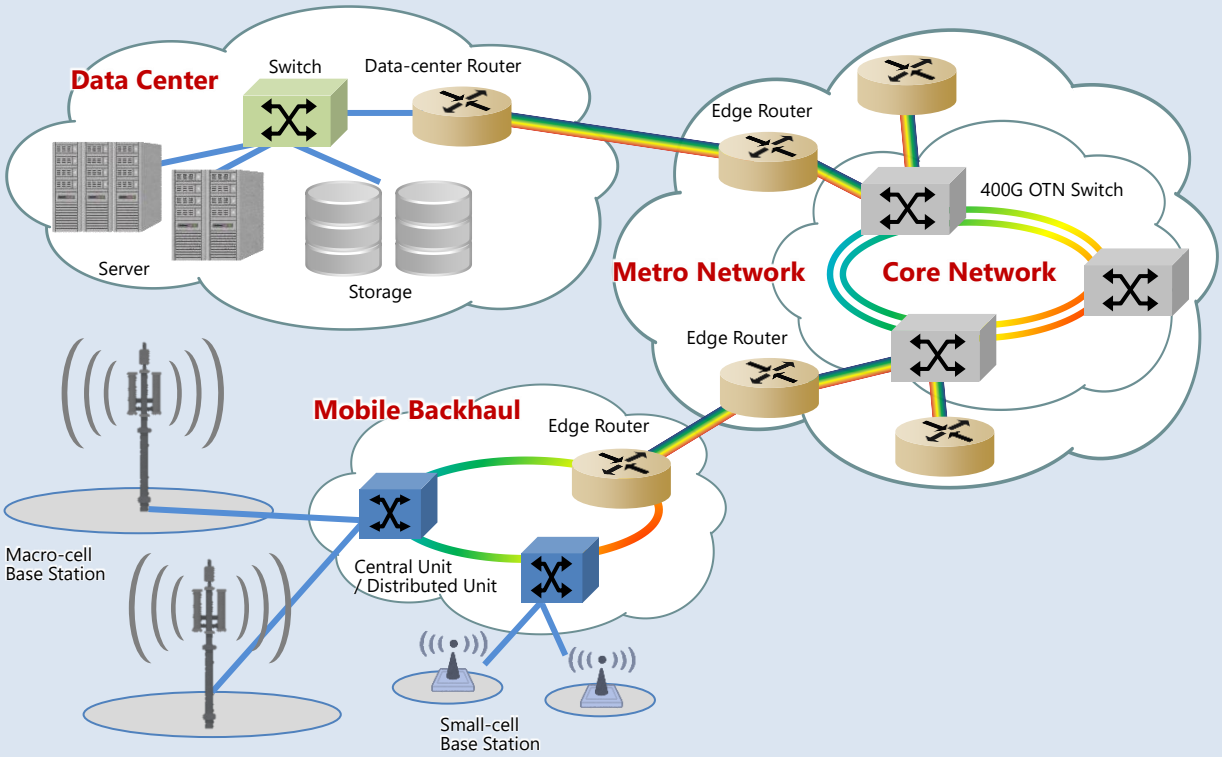


Figure 1. 5G Network Schematic

**Optical network market**

The core and metro networks that connect 5G base stations and data centers are composed of an optical network connected by optical fibers. With the deployment of 5G, optical transmission technology for high-efficiency, high-capacity communications have been developed and put into practical use. Additionally, links between datacenters, also known as Data Center Interconnect (DCI), are leveraging 100G, 200G,and 400G connections, and the 400G coherent DWDM (Dense Wavelength Division Multiplexing) interface 400ZR has been standardized and 800ZR is being developed now. 400GbE using PAM4 has been standardized and 800 Gbps speed 100G PAM-4 PHY is started to release for client-side transmission as well. Figure 2 shows DWDM port unit shipments, including 400ZR and 800G. In the future, 400ZR, 800ZR and PAM4 are expected to expand in the optical network market as 5G spreads.

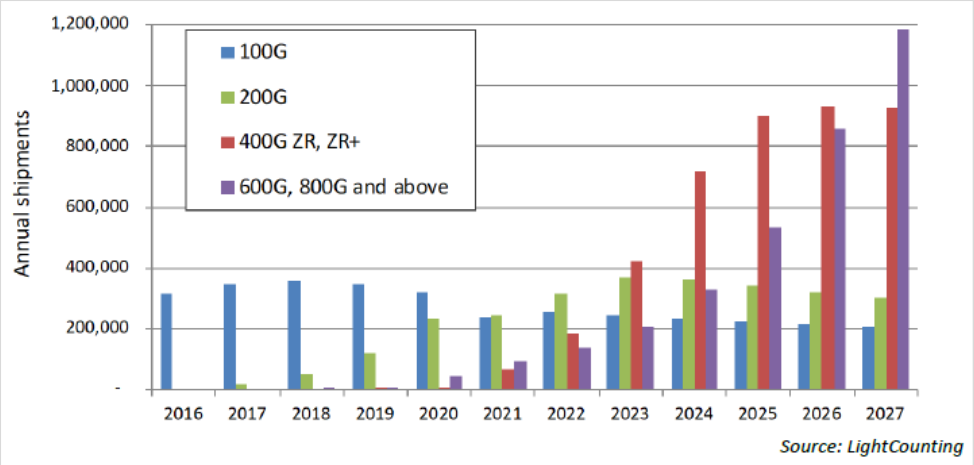


Figure 2. DWDM Port Unit Shipments Forecast

**5G base station market**

To increase the network capacity, it is essential to also increase base station data throughput. The technology that contributes most to increasing the capacity of 5G wireless networks is the expansion of the frequency bandwidth. It is now possible to expand the frequency bandwidth by using a carrier frequency higher than LTE. The maximum frequency bandwidth per channel of LTE was 20 MHz, but with 3GPP Release 15, the maximum frequency bandwidth in 5G has expanded to 100 MHz for FR1 (carrier frequency: 410 MHz to 7,125 MHz) and to 400 MHz for FR2 (carrier frequency: 24.25 GHz to 52.6 GHz). The total number of units shipped in the base station market is trending flat as shown in Figure 3, but shipments of 5G base stations are expected to grow due to the switch from LTE.

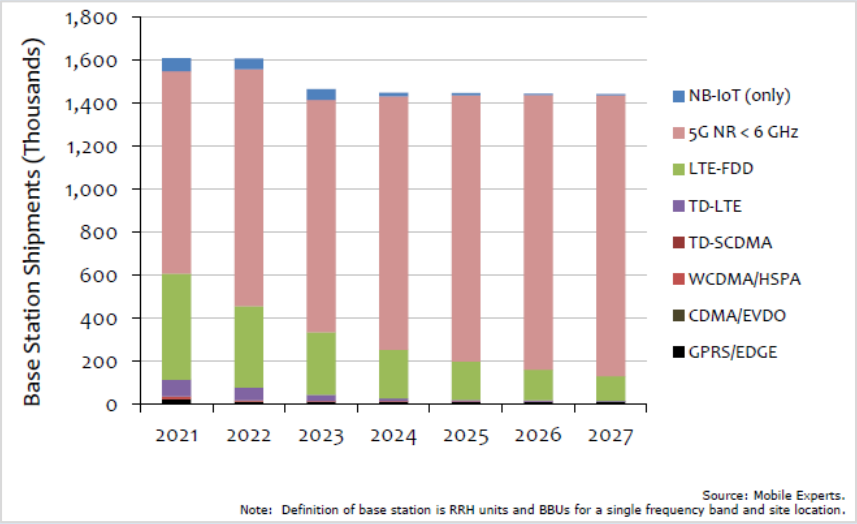


Figure 3. Base Station Market Forecast

## Required Specifications for Communications Systems and Reference Clocks for 5G

### PAM4

Historically, NRZ transmissions using on/off keying have been widely used in optical communications due to their simplicity. More recently, a pulse amplitude modulation technique, PAM4 has been adopted PAM4 uses multiple amplitude levels to code two bits simultaneously. This makes it possible to secure twice the transmission speed as NRZ.

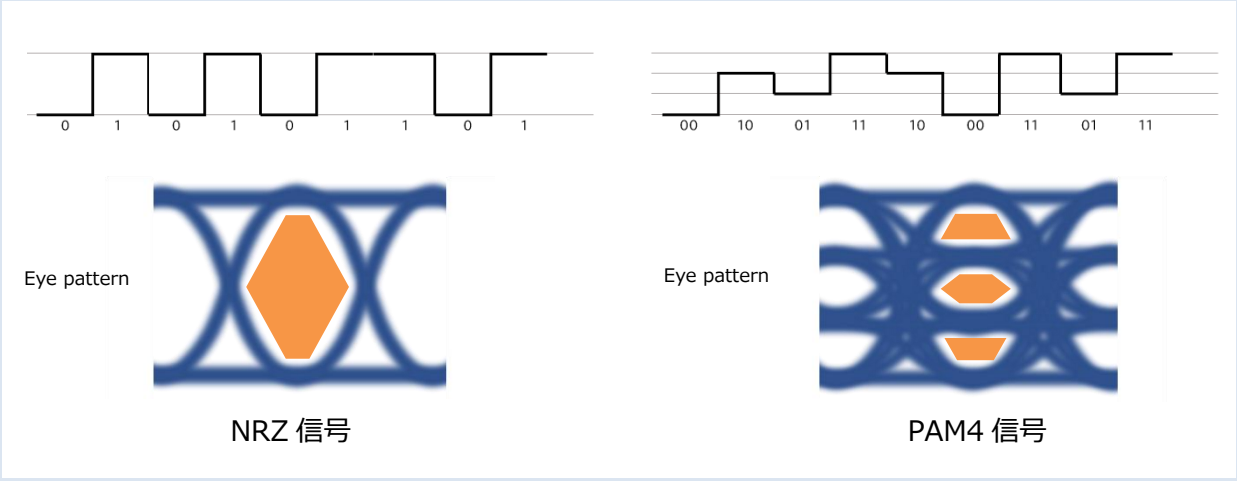


Figure 4. NRZ and PAM4 Signals

Compared to the NRZ (Non-Return-to-Zero) signal, the PAM4 signal has smaller eye openings (orange parts in the figure) as observed using eye patterns, and the quality of transmitted signals tends to deteriorate. To ensure the quality of the transmission signal, a SPXO (Simple Packaged Crystal Oscillator) with low jitter performance is required for the reference clock. About 100 fs is pervasive in the market as a jitter threshold for the reference clock. Also, due to the modularization of optical communication units, reference clocks must be small and consume low current.

### 400ZR

400ZR uses coherent optical transmission technology to reach speeds up to 400 Gbps across long distances. Unlike NRZ or PAM4, 400ZR uses quadrature modulation, performed by a digital coherent signal processing circuit, and the modulated data is transmitted on the coherent light.

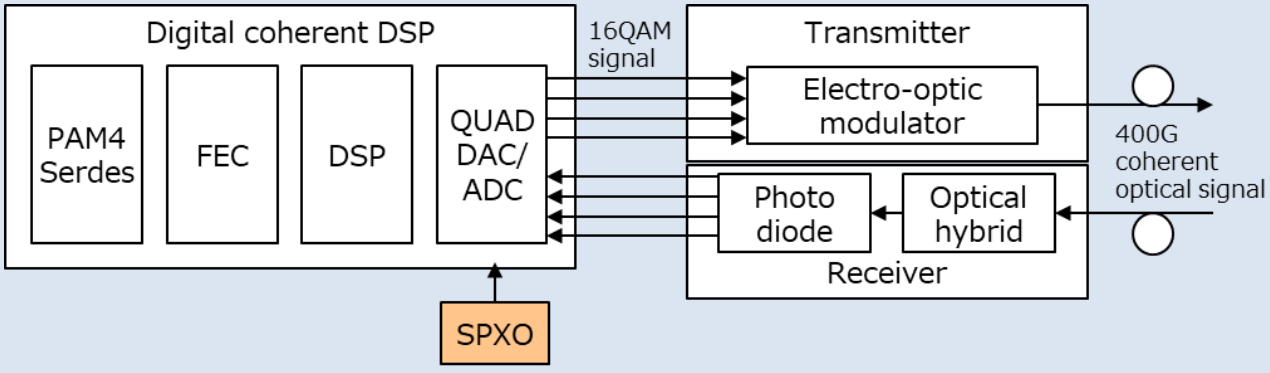


Figure 5. 400ZR Block Diagram

To process 400G signals, the sampling clock required for the DAC/ADC of the signal processing circuit requires an SPXO with frequencies often between156.25 MHz and 500 MHz, and low jitter characteristics of around 100 fs. In addition, the frequency tolerance is specified by OIF-400ZR-01.0, and an accuracy of ± 20 x $10^{-6}$ is required. Low power is needed for the entire system, and there is a strong preference for clocks with low current consumption characteristics.

**5G wireless base station, RU (Radio Unit)**

In 5G wireless base stations, complex techniques such as QAM(quadrature amplitude modulation) and OFDM (orthogonal frequency division multiplexing) are used to maximize throughput for a given channel of wireless spectrum.

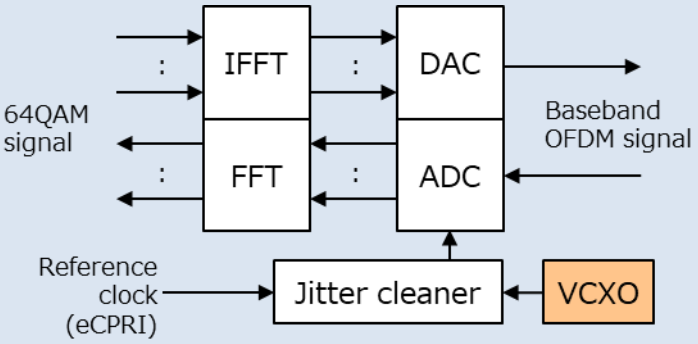


Figure 6. OFDM Block Diagram

Along with faster transmission speeds due to expansion of frequency bandwidth, DAC/ADC in OFDM of 5G systems requires a faster and more accurate sampling clock than LTE. Therefore, VCXOs (voltage controlled crystal oscillators) for Jitter Cleaner require high frequency and low jitter characteristics. In recent years, the technology for using SPXO as the reference clock of Jitter Cleaner has gradually entered practical use. Even so, however, SPXOs must have high frequency and low jitter characteristics. In addition, since base stations are installed outdoors where they are exposed to vibrations in the surrounding environment, a clock whose characteristics are stable when exposed to vibration is required; that is, a clock with a small acceleration sensitivity is required.

**Technology for Realizing High-Frequency Clocks**

SPXO or VCXO are generally used for high-frequency clocks of 100 MHz or higher, and they are configured such that the oscillator and IC are built in one package. There are several types of technologies for realizing high-frequency clocks. These technologies are integrated with built-in crystal units or an IC. Here, technologies for realizing high-frequency clocks and their characteristics are shown.

- Fundamental mode oscillator: High-frequency crystal unit + fundamental oscillation circuit (IC)

  In an ordinary quartz crystal unit, the quartz is cut out at what is called an AT cut angle and is processed into a thin crystal chip according to the frequency. The higher the frequency, the thinner it needs to be processed. A 100-MHz crystal unit has a thickness of 16.7 µm. A stable high-frequency clock with low noise and low jitter can be obtained by combining the crystal unit with a high-frequency oscillator circuit. On the other hand, since the crystal chip is thin, it has low mechanical strength and is vulnerable to vibration.

- 3rd overtone mode oscillator: 3rd overtone mode crystal unit + 3rd overtone oscillator circuit (IC)

  In addition to fundamental mode vibration, crystal units have other odd number harmonics, such as the third and fifth. Third overtone crystal units resonate at the third harmonic mode. In other words, a 100-MHz third-overtone mode crystal unit has the same thickness (50.1 µm) as a 33.3333 MHz crystal unit. This relatively greater thickness increases mechanical strength and makes the crystal less susceptible to damage from vibration. It also has low noise and jitter characteristics comparable to those of a fundamental mode oscillator. However, the equivalent series resistance is large at the third harmonic, increasing the oscillation circuit design difficulty,

and the fundamental wave oscillates depending on the operating environment, which may cause a fatal problem in system operation. In addition, since the Q value is high, the frequency does not easily change even if the load capacitance of the oscillation circuit is changed, so it is not suitable for VCXO.

- HFF (high-frequency fundamental) oscillator: HFF crystal unit + fundamental oscillation circuit (IC)
  HFF crystal oscillators are able to vibrate at high frequencies because they have an inverted-mesa structure that is created by using a photolithographic process to etch only the vibration area of the crystal chip to an extreme thinness. Since the crystal chip is adequately thick in areas outside the vibration area, it has high mechanical strength and is resistant to vibration. A stable high-frequency clock with low noise and low jitter can be obtained by combining the crystal unit with a high-frequency oscillator circuit.

- PLL oscillator: Low-frequency crystal unit + fundamental oscillation circuit & PLL circuit (IC)
  PLL oscillators use a low-frequency crystal unit that is resistant to mechanical stress and vibration as the crystal unit. The frequency obtained by the oscillation circuit is multiplied by the PLL circuit to achieve higher frequencies. While the PLL circuit can generate a high-frequency clock relatively easily, it increases noise, so its jitter characteristics are inferior to those of other technologies. The current consumption tends to increase as the PLL circuit is driven.
  A MEMS (micro electro-mechanical system) oscillator uses a MEMS resonator instead of a quartz crystal resonator.

- SAW (surface acoustic wave) oscillator: SAW resonator + fundamental oscillation circuit (IC)
  A SAW resonator is a device that generates surface acoustic waves on the surface of a crystal chip and resonates with it. The characteristics of a SAW resonator are determined not by the thickness of the crystal chip but by the distance between the comb-shaped electrodes (interdigital transducers: IDT) formed on the crystal surface. Frequencies can be increased up to about 1 GHz by using a photolithographic process to form electrodes and produce crystal chips that are thick and have high mechanical strength. Noise during oscillation is also low, and low jitter characteristics can be obtained. On the other hand, whereas the frequency/temperature coefficient of the crystal unit exhibits third-order characteristics, the SAW resonator exhibits second-order characteristics, so the frequency stability is low.

Table 1 summarizes the foregoing high-frequency technologies and their features.

Table 1. Technologies for High-Frequency Clocks and Their Characteristics

| | | Fundamental mode oscillator | 3rd overtone mode oscillator | HFF oscillator | PLL oscillator (MEMS oscillator) | SAW oscillator |
|---|---|---|---|---|---|---|
| Technology | Crystal unit | High-frequency crystal unit | 3rd overtone mode crystal unit | HFF crystal unit | Low-frequency crystal unit or MEMS crystal unit | SAW resonator |
| | IC | Fundamental mode oscillator circuit | 3rd overtone mode oscillator circuit | Fundamental mode oscillator circuit | Fundamental mode oscillator circuit + PLL circuit | Fundamental mode oscillator circuit |
| Characteristics | Low noise & jitter | ✓✓✓ | ✓✓✓ | ✓✓✓ | ✓ | ✓✓✓ |
| | Resistant to vibration & shocks | ✓ | ✓✓✓ | ✓✓✓ | ✓✓✓ | ✓✓✓ |
| | Low current consumption | ✓✓✓ | ✓✓✓ | ✓✓✓ | ✓✓ | ✓✓ |
| | High operating reliability | ✓✓✓ | ✓ | ✓✓✓ | ✓✓ | ✓✓✓ |
| | High frequency stability | ✓✓✓ | ✓✓✓ | ✓✓✓ | ✓✓✓ | ✓ |
| | Suited to VCXO design | ✓✓✓ | ✓ | ✓✓✓ | ✓✓✓ | ✓✓ |

Of the various technologies that are available, Seiko Epson has chosen to use HFF oscillators to successfully commercialize high-frequency clocks that match the needs of the 5G communication systems market.

**Epson HFF Crystal Oscillator Characteristics**

As mentioned above, HFF oscillators have a configuration in which the HFF crystal and the fundamental mode oscillator circuit (IC) are contained in one package. The built-in HFF crystal can vibrate at a high frequency because the crystal chip has been through a photolithographic process that creates an inverted-mesa structure in which only the vibration area of the crystal chip is made extremely thin.

The relationship between the oscillation frequency *F* [MHz] of the crystal unit and the thickness *t* [µm] of the vibration area of the crystal chip is described by the following equation:

$$F = 1{,}670/t$$

To obtain an oscillation frequency of 80 MHz to 500 MHz, it is necessary to process the vibration area so that it has a thickness of between 3 µm and 20 µm. However, in the inverted mesa structure, the areas outside the vibration area are sufficiently thick. Epson's products have a thickness of 80 µm. This is equivalent to the thickness of a crystal chip that has an oscillation frequency of 21 MHz, has mechanical strength equivalent to that of an ordinary crystal unit, and has the advantage of being resistant to vibration.

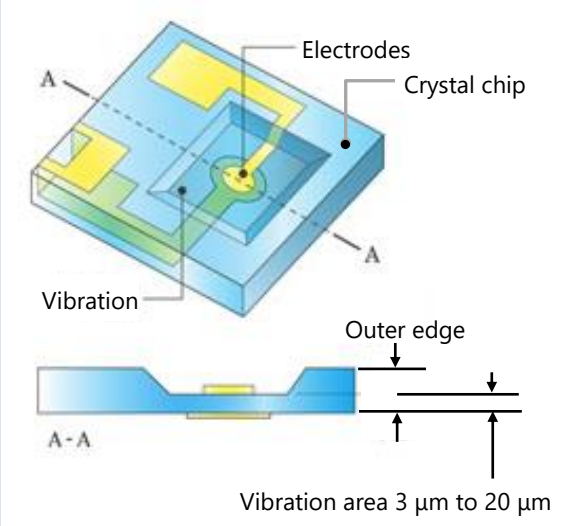


Figure 7. HFF Crystal Unit

- Shock and vibration performance

Our products are subjected to impact and vibration tests during reliability testing. The figure below shows the impact and vibration test results of our 491.52-MHz HFF SPXO SG3225EEN. It cleared the in-house standard for frequency fluctuation of ± 10 ppm max. under the standard conditions of 1,000 G in the impact test and 20 G in the vibration test. Furthermore, even when vibrations and shocks exceeding the standard conditions were applied, there was no failure attributable to HFF oscillator damage, and there was no abnormality in the frequency fluctuation. This result attests to the fact that the HFF oscillator has high shock and vibration performance at the upper limit of 500 MHz.

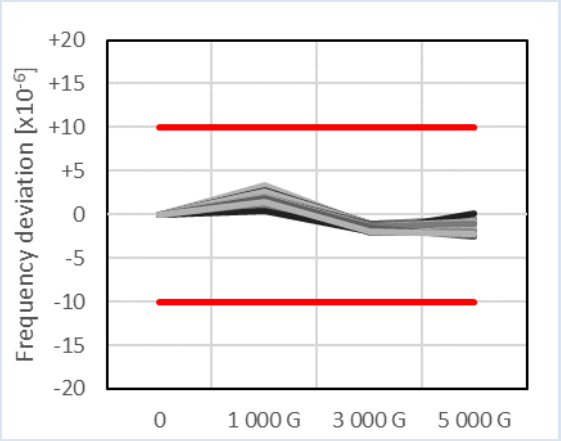


Figure 8. SG3225EEN 491.52 MHz Shock Test Results

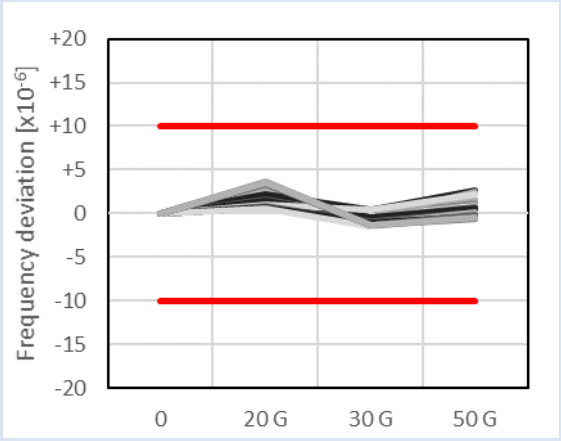


Figure 9. SG3225EEN 491.52 MHz Vibration Test Results

- Acceleration sensitivity (G-sensitivity)

As previously stated, since base stations are installed outdoors where they are exposed to vibrations in the surrounding environment, a clock whose frequency changes little when exposed to vibration, i.e., a clock with a small acceleration sensitivity, is required. At Epson, the crystal chip shape that has the least impact on characteristics during vibration is simulated via eigenvalue analysis, and the optimum design is performed by trial verification. The figure below shows the G sensitivity of an Epson 122.88-MHz HFF VCXO VG7050VFN. A low acceleration sensitivity of 2 x $10^{-9}$/g is achieved.

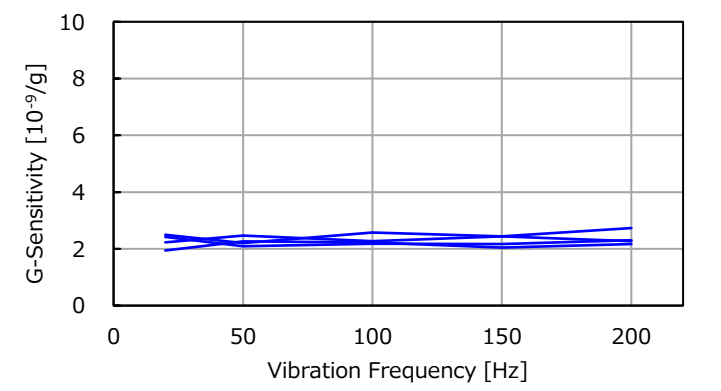


Figure 10. 122.88-MHz VG7050VFN G Sensitivity

- Frequency/temperature coefficient

For 400ZR, a clock frequency tolerance of ± 20 x $10^{-6}$ Max. is required. This is impossible to achieve with an ordinary crystal oscillator because the frequency/temperature coefficient alone exceeds ± 20 x $10^{-6}$ between -40°C and + 85°C. Epson's HFF SPXO SG2520VHN offers the characteristics shown in the figure below because Epson has incorporated a temperature compensation circuit in the IC. This satisfies the requirements of 400ZR.

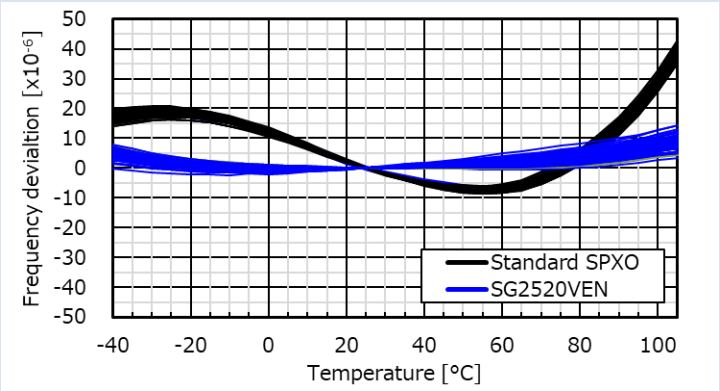


Figure 11. Frequency/Temperature Coefficient of an Ordinary Crystal Oscillator vs a SG2520VHN

- Phase noise, Phase jitter, PSNR (power supply noise rejection) characteristics

Epson's HFF oscillator uses an HFF crystal unit to achieve stable high frequency oscillation up to 500 MHz with low noise and low jitter. In addition, the built-in Epson IC has a carefully considered low-noise design that has been optimized using simulation. The figure below shows the phase noise characteristics of Epson's 491.52-MHz HFF SPXO SG2520VHN and 491.52-MHz HFF VCXO VG3225VFN. Both have excellent phase noise and phase jitter characteristics.

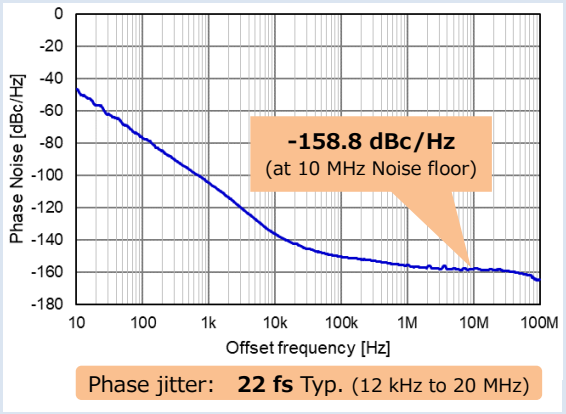


Figure 12. SG2520VHN 491.52 MHz Phase Noise Characteristics

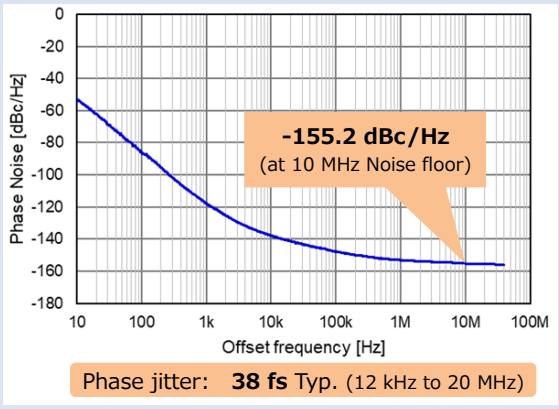


Figure 13. VG3225VFN 491.52 MHz Phase Noise Characteristics

In actual applications, the power supply voltage applied to the oscillator contains noise, and this noise causes deterioration of the oscillator's phase noise and phase jitter characteristics. For example, when the power supply voltage contains noise having a frequency component of 10 kHz, spurs are ~~spurious(spurs?) is~~ generated near the offset frequency of 10 kHz of the phase noise characteristic. Epson's HFF SPXO uses a low noise LDO (low dropout) that stabilizes the power supply voltage, reduces noise, and limits the deterioration of phase noise and phase jitter characteristics. The figure below shows the phase jitter characteristics, that is, the PSNR characteristics, when noise is superimposed on the power supply voltage of a SG2520EHN and an equivalent product from a competitor. The noise model was a sine wave with frequencies from 20 kHz to 5 MHz and a level of 50 mVp-p. It can be confirmed that the deterioration of the phase jitter characteristics of the SG2520EHN is limited.

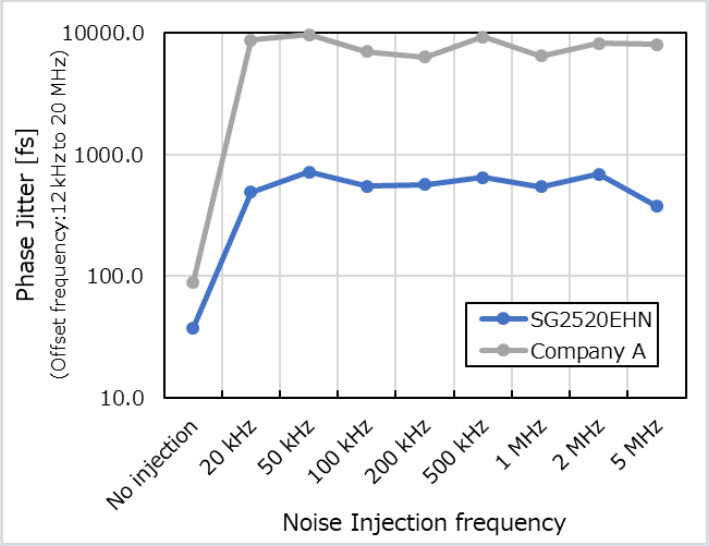


Figure 14. PSNR Characteristics of the SG2520EHN and a Competitor's Product

## Detailed Specifications of Epson HFF Oscillators

The detailed specifications of our HFF oscillators (SPXO / VCXO), which have characteristics that match the needs of the 5G communication systems market, are shown below.

- HFF SPXO: SG2016EHN/SG2520EHN, SG2016VHN/SG2520VHN specifications

| Item | Symbol | Specifications | | | Conditions | | |
|---|---|---|---|---|---|---|---|
| | | LV-PECL | LVDS | | | | |
| | | SG2016EHN SG2520EHN | SG2016VHN SG2520VHN | | | | |
| Output frequency range | fo | 25 MHz to 500 MHz | | | Please inquire for information about supported frequencies. | | |
| Supply voltage | $V_{CC}$ | D: 2.5 V ± 5%<br>C: 3.3 V ± 5% | E: 1.8 V ± 5% | D: 2.5 V ± 5%<br>C: 3.3 V ± 5% | | | |
| Storage temperature range | T_stg | -55 °C to +125 °C | | | | | |
| Operating temperature range | T_use | G: -40 °C to +85 °C, H: -40 °C to +105 °C | | | | | |
| Frequency tolerance | f_tol | C: ±20 × $10^{-6}$ Max. | | | Including frequency tolerance, frequency/temperature coefficient, supply voltage variation, 10-year aging (+25°C) | | |
| Current consumption | $I_{CC}$ | 60 mA Max. | – | | OE or $\overline{ST}$ = $V_{CC}$, L_ECL = 50 Ω | | |
| | | – | 25 mA/–/25 mA Max. | 25 mA/30 mA/25 mA Max. | OE or $\overline{ST}$ = $V_{CC}$, Output options: A/B/C | 25 MHz ≤ fo < 212 MHz | |
| | | | | 28 mA/35 mA/28 mA Max. | | 212 MHz ≤ fo < 392 MHz | |
| | | | | 28 mA/35 mA/30 mA Max. | | 392 MHz ≤ fo ≤ 500 MHz | |
| Output disable current | I_dis | 35 mA Max. | 20 mA Max. | | OE = GND | | |
| Standby current | I_std | 30 µA Max. | | | $\overline{ST}$ = GND | | |
| Symmetry | SYM | 45% to 55% | | | At output crossing point | | |
| Output voltage (LV-PECL) | $V_{OH}$ | $V_{CC}$ - 1.1 V Min. | – | | Output options: A | | DC characte r-istics |
| | $V_{OL}$ | $V_{CC}$ - 1.5 V Max. | | | | | |
| Output voltage (LVDS) | $V_{OD}$ | – | 250 mV to 450 mV | | Output options: A | Differential output voltage $V_{OD1}$, $V_{OD2}$ | |
| | | | – | 200 mV to 500 mV | Output options: B | | |
| | | | 300 mV to 600 mV | | Output options: C | | |
| | $dV_{OD}$ | – | 50 mV Max. | | $dV_{OD}$ = \| $V_{OD1}$ - $V_{OD2}$ \| | | |
| | $V_{OS}$ | – | 0.65 V to 0.85 V | 1.15 V to 1.35 V | Offset voltage, $V_{OS1}$, $V_{OS2}$ | | |
| | $dV_{OS}$ | – | 50 mV Max. | | $dV_{OS}$ = \| $V_{OS1}$ - $V_{OS2}$ \| | | |
| Output load condition | L_ECL | 50 Ω | – | | $V_{CC}$ - 2.0 V termination | | |
| | L_LVDS | – | 100 Ω | | Output options: A, C | Connection between OUT - $\overline{OUT}$ | |
| | | | 50 Ω | | Output options: B | | |
| Input voltage | $V_{IH}$ | 70 % $V_{CC}$ Min. | | | OE or $\overline{ST}$ terminal | | |
| | $V_{IL}$ | 30 % $V_{CC}$ Max. | | | | | |
| Rise time / fall time | tr/tf | 0.35 ns Max. | | | LV-PECL: 20 % - 80 % ($V_{OH}$ - $V_{OL}$)<br>LVDS: 20 % - 80 % differential output peak to peak | | |
| Oscillation startup time | t_str | 10 ms Max. | | | t = 0 at 90 % $V_{CC}$ | | |
| Phase jitter | $t_{PJ}$ | 250 ps Max.<br>200 ps Typ. | 400 ps Max.<br>300 ps Typ. | 250 ps Max.<br>170 ps Typ. | fo < 100 MHz | | Offset frequency<br>fo < 50 MHz:<br>12 kHz to 5 MHz<br>fo ≥ 50 MHz:<br>12 kHz to 20 MHz |
| | | 90 ps Max.<br>70 ps Typ. | 130 ps Max.<br>100 ps Typ. | 100 ps Max.<br>70 ps Typ. | 100 MHz ≤ fo ≤ 156 MHz | | |
| | | 70 ps Max.<br>40 ps Typ. | 70 ps Max.<br>50 ps Typ. | 60 ps Max.<br>40 ps Typ. | 156 MHz < fo ≤ 212 MHz | | |
| | | 60 ps Max.<br>30 ps Typ. | 60 ps Max.<br>35 ps Typ. | 50 ps Max.<br>25 ps Typ. | 212 MHz < fo ≤ 391 MHz | | |
| | | 50 ps Max.<br>25 ps Typ. | 60 ps Max.<br>30 ps Typ. | 50 ps Max.<br>20 ps Typ. | fo > 391 MHz | | |
| Dimensions | - | 2.0 x 1.6 x 0.63 mm | | | SG2016EHN/SG2016VHN | | |
| | | 2.5 x 2.0 x 0.74 mm | | | SG2520EHN/SG2520VHN | | |

Detailed information on the above products is available on our website. Please click on the links below.

Product page SG2016EHN SG2520EHN (LV-PECL output)

SG2016VHN SG2520VHN (LVDS output)

Video content presenting the competitive advantages of HFF

- HFF VCXO: VG3225EFN/VG5032EFN/VG7050EFN, VG3225VFN/VG5032VFN/VG7050VFN specifications

| Item | Symbol | Specifications | | Conditions | |
|---|---|---|---|---|---|
| | | LV-PECL | LVDS | | |
| | | VG3225EFN<br>VG5032EFN<br>VG7050EFN | VG3225VFN<br>VG5032VFN<br>VG7050VFN | | |
| Output frequency range | fo | 25 MHz to 500 MHz<br>(*250 MHz < fo ≤ 500 MHz planned for release in the near future) | | Please inquire for information about supported frequencies. | |
| Supply voltage | $V_{CC}$ | C: 3.3 V ± 0.165 V | | | |
| Control voltage | Vc | 1.65 V ±1.65 V | | | |
| Storage temperature range | T_stg | -55 · C to +125 · C | | | |
| Operating temperature range | T_use | G: -40 · C to +85 · C, H: -40 · C to +105 · C | | | |
| Frequency tolerance | f_tol | J: ±50 × $10^{-6}$ Max. | | Except the following: | Including frequency tolerance, frequency/temperature coefficient, supply voltage variation, 10-year aging (+25°C) at Vc = 1.65 V |
| | | V: ±60 × $10^{-6}$ Max. | | VG3225EFN/VFN,<br>T_use: H, fo > 250 MHz | |
| Absolute pull range | APR | B: ±50 × $10^{-6}$ Min. | | 25 MHz ≤ fo ≤ 42.5 MHz,<br>50 MHz ≤ fo ≤ 85 MHz,<br>100 MHz ≤ fo ≤ 170 MHz | T_use: G or H |
| | | M: ±20 × $10^{-6}$ Min. | | 25 MHz ≤ fo ≤ 250 MHz | T_use: G or H |
| | | | | 250 MHz < fo ≤ 420 MHz | T_use: G |
| | | S: ±10 × $10^{-6}$ Min. | | Total frequency band | T_use: G |
| Current consumption | $I_{CC}$ | 60 mA Max. | 25 mA Max. | OE = $V_{CC}$, L_ECL = 50 Ω or L_LVDS = 100 Ω | |
| Output disable current | I_dis | 25 mA Max. | 15 mA Max. | OE = GND | |
| Input impedance | Zin | 10 MΩ Min. | | DC level | |
| Frequency change polarity | - | Positive slope | | $V_C$ = 0 V to 3.3 V | |
| Symmetry | SYM | 45% to 55% | | At output crossing point | |
| Output voltage (LV-PECL) | $V_{OH}$ | $V_{CC}$ - 1.1 V Min. | – | DC characteristics | |
| | $V_{OL}$ | $V_{CC}$ - 1.5 V Max. | – | | |
| Output voltage (LVDS) | $V_{OD}$ | – | 250 mV to 450 mV | Differential output voltage, $V_{OD1}$, $V_{OD2}$ | DC characteristics |
| | $V_{OS}$ | – | 1.15 V to 1.35 V | Offset voltage, $V_{OS1}$, $V_{OS2}$ | |
| LVPECL load condition | L_ECL | 50 Ω | – | $V_{CC}$ - 2.0 V termination | |
| LVDS load condition | L_LVDS | – | 100 Ω | Connection between OUT - $\overline{OUT}$ | |
| Input voltage | $V_{IH}$ | 70 % $V_{CC}$ Min. | | OE terminal | |
| | $V_{IL}$ | 30 % $V_{CC}$ Max. | | | |
| Rise time / fall time | tr/tf | 0.5 ns Max. | 0.3 ns Max. | LV-PECL: 20 % - 80 % ($V_{OH}$ - $V_{OL}$)<br>LVDS: 20 % - 80 % differential output peak to peak | |
| Oscillation startup time | t_str | 10 ms Max. | | Time at minimum supply voltage is 0 | |
| Phase jitter | $t_{PJ}$ | 120 fs Max. | 160 fs Max. | fo = 122.88 MHz | Offset frequency: 12 kHz to 20 MHz |
| | | 80 fs Max. | 80 fs Max. | fo = 245.76 MHz | |
| | | 70 fs Max. | 80 fs Max. | fo = 500.00 MHz | |
| G-sensitivity | Gs | 2 × $10^{-9}$/g Typ., 4 × $10^{-9}$/g Max. | | Vibration frequency: 20 Hz to 200 Hz | |
| Dimensions | - | 3.2 x 2.5 x 1.05 mm | | VG3225EFN/VG3225VFN | |
| | | 5.0 x 3.2 x 1.30 mm | | VG5032EFN/VG5032VFN | |
| | | 7.0 x 5.0 x 1.50 mm | | VG7050EFN/VG7050VFN | |

Detailed information on the above products is available on our website. Please click on the links below.

Product page VG3225EFN VG5032EFN VG7050EFN (LV-PECL output)
VG3225VFN VG5032VFN VG7050VFN (LVDS output)

**Conclusion**

HFF oscillators are the best reference clock for 5G communication systems and help to maximize the value of customers' products.

Seiko Epson will continue to recommend crystal devices that enrich society.