# Circuit Design for Crystal Oscillators and Crystal Units Peripheral Circuits

[1] Preface

During the design and layout of electronic devices and communications systems, careful consideration must go into the crystal oscillator and peripheral circuits in order to optimize performance. As the core of the signal source, the crystal oscillator must generate a high precision output, and is therefore inherently sensitive to high frequency noise from the rest of the board.

This circuitry requires explicit care during design. These Technical Notes serve as a design guide for reducing noise in several peripheral circuits where high frequency noise can be particularly harmful to the crystal oscillator output.

In addition, it explains notes on designing peripheral circuits for crystal units.

[2] Crystal oscillators peripheral circuits

[Source of noise in crystal oscillators and peripheral circuits]

First, in Figure 1 we indicate the typical types of noise generated from crystal oscillators and the peripheral circuits. There are three main noise sources:

1. Noise from power line
2. Noise from output line
3. Noise from crystal oscillator

What generally is referred to as “noise” is the cumulative result of these three factors. Below we provide an explanation to address each type of noise.

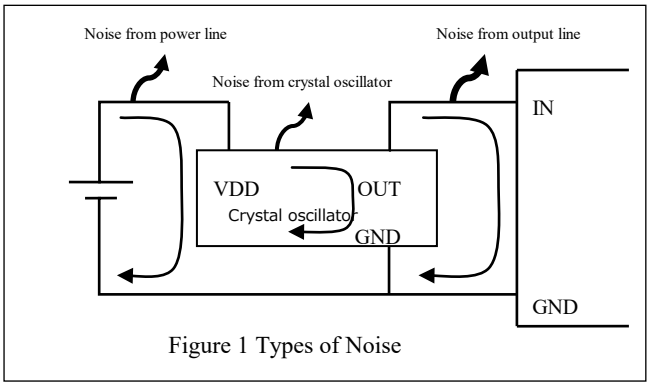



Figure 1 Types of Noise

1. Noise from power line

Voltage ripple and switching noise are commonly emitted by the power line trace. This noise can affect the output of the crystal oscillator. Furthermore, it is necessary to ensure that ripple noise produced by the crystal oscillator does not flow to the power line. Implementing such countermeasures also improve isolation to prevent external noise produced by other devices from flowing to the crystal oscillator, which guarantees the stability of the crystal oscillator.

2. Output line noise

Output line noise refers to signals output by the crystal oscillator where the output line acts as an antenna. Noise reducing techniques should be implemented for both the output signal and the physical trace.

3. Crystal oscillator IC noise

Crystal oscillator IC noise refers to noise emitted by the internal IC and wiring of the crystal oscillator. Addressing this noise requires ensuring a stable power supply to the crystal oscillator and ensuring the formation of the required waveform to achieve stable operation of the crystal oscillator. These noise sources are dependent on the causes above and can be mitigated indirectly with power line and output line techniques mentioned later in the paper.

The level of noise emitted from the sources above is proportionate to the electrical current and the current loop path. Therefore, a decrease in the electrical current or current loop path impedance will result in a reduced level of noise emitted.
In general, the following type of correlation exists between electrical current and current loop path length as it relates to crystal oscillators and their peripheral circuits.

Electrical current volume: Power line = crystal oscillator > output line
Current loop size: Output line > power line >> crystal oscillator

Output line noise has the largest effect on the crystal oscillation circuitry, followed by the noise contribution of the power line. The level of noise emitted by the actual crystal oscillator IC is typically far less in comparison to noise from the other two sources.

[Noise countermeasures]

Thus far in these Technical Notes, we have examined the sources of noise in crystal oscillators and their peripheral circuits. Here, we explain measures for reducing this noise. There are three main noise reduction measures:

1. Establish stable power and ground connections.
2. Mount a filter to prevent noise from the power line.
3. Configure a stable output line on the board.

1. Stable power and ground connections

Stable power and ground connection refers to an extremely low level of impedance across a broad frequency band (particularly high frequencies) as well as a conductor that achieves uniform potential across all points of the bandwidth. In particular, the ground line represents the base potential for a circuit and thus must achieve the greatest level of stability. This requires the design of a ground plane that has a broad surface area with no constriction. On a multi-layered board, extra ground planes are used to configure the power line and ground line on independent layers. When the design involves solder joints, broader contact area ensures lower impedance, and therefore less noise. Do not route any signal lines, supply voltage lines, or GND lines underneath the area where the oscillators are mounted including any internal layers and on the opposite side of the board.

2. Power line filtering

It is common practice to place a filter between power and ground lines to prevent noise from the crystal oscillator from leaking into the power or ground lines and conversely to prevent noise from the power line into the crystal oscillator. Typically, a bypass capacitor is used as a filter for the power line and ground line. A detailed explanation is provided below.

a. Bypass capacitor

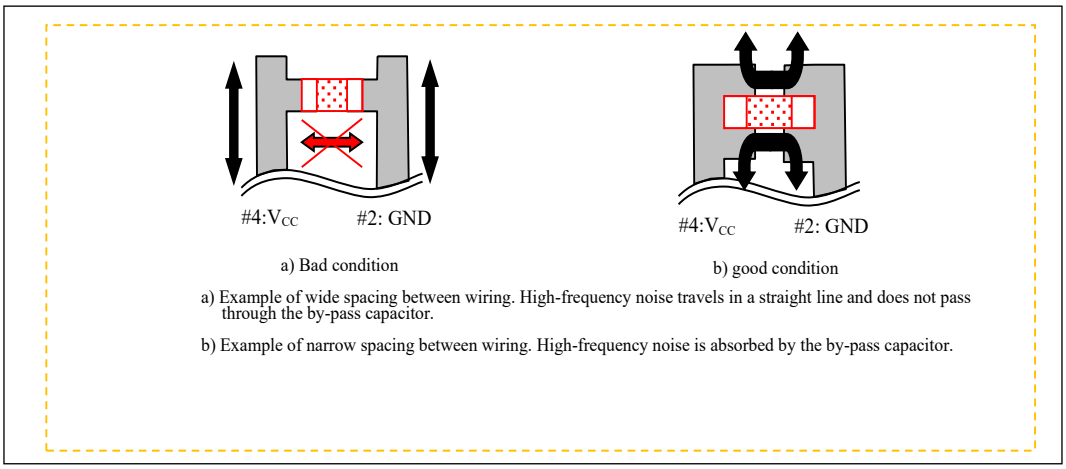
A bypass capacitor works to lower interacting electrical impedance and help stabilize circuit operation while absorbing noise that exists on the power line. This is a commonly known noise elimination method. Mounting a capacitor with the appropriate capacitance value will resolve the majority of noise-related issues.

i. Bypass capacitor capacity value

The standard bypass capacitance values are between 0.01µF and 1µF. This value should be set as low as possible but within a range where the power terminal $V_{CC}$ and power line impedance in relation to the ground is a frequency that is three times the frequency of the crystal oscillator. Here, you must confirm the frequency properties at this capacity to ensure that impedance levels on the high-frequency side or low-band side do not increase.

ii. Mounting a by-pass capacitor

To minimize noise, the bypass capacitor should be mounted as close to the crystal oscillator as possible. As the trace length grows, parasitic inductance will increase and cause increased impedance for higher frequencies. The trace length of the bypass capacitor should be configured so that the signal passes through the connection to the power line. This will force noise to pass through the bypass capacitor and improve the noise elimination effect.
Avoid the type of formation indicated in Figure 2a. when mounting the bypass capacitor. High-frequency noise typically travels in a straight line so noise will not pass through the bypass capacitor if using a pattern like that shown in Figure 2b.

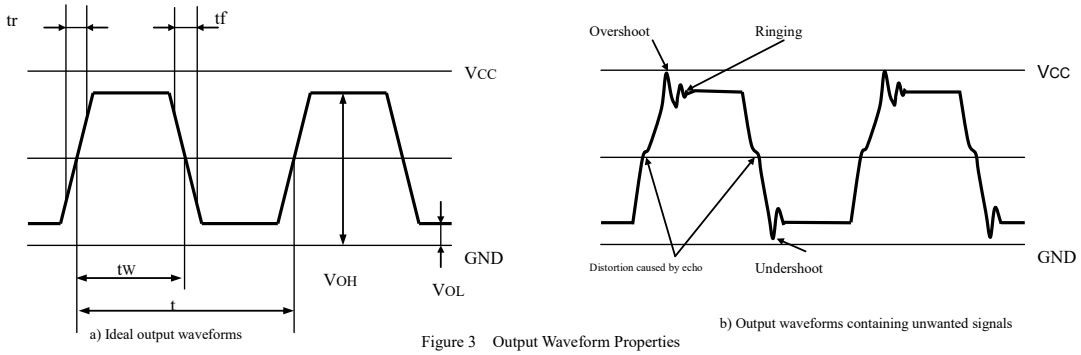



a) Example of wide spacing between wiring. High-frequency noise travels in a straight line and does not pass through the by-pass capacitor.

b) Example of narrow spacing between wiring. High-frequency noise is absorbed by the by-pass capacitor.

3. Configuring a stable output line

A stable output line refers to a trace that can efficiently transfer the output waveform of the crystal oscillator to the desired input with minimal distortion and electromagnetic emissions.
The key to configuring a stable output line involves ensuring the waveform properties, such as $t_r$, $t_f$, $V_{OH}$, $V_{OL}$, etc, required at the input. Furthermore, a stable output line requires the elimination of unwanted signals such as the overshoot, undershoot, ringing, and echo, as seen in Figure 3b. It is also important to be aware of the antenna efficiency of the trace to minimize unwanted radiations.




a) Ideal output waveforms

b) Output waveforms containing unwanted signals

Figure 3 Output Waveform Properties

Measures for preventing output waveform distortion include:

a. Configure serial resistance
b. Configure termination resistance
c. Configure a filter
d. Matching output line impedance

a. Configuring serial resistance

Connecting a crystal oscillator to an input device normally results in the production of waveform distortions including overshoot, undershoot, and ringing. These distortions contain high-frequency elements that are 3-7 times higher than the oscillation frequency and result in the emission of noise that should be eliminated. To eliminate such distortions, serial resistance is connected between the output terminal of the crystal oscillator and the output line as shown in Figure 4. The resistance value is configured so that the sum of the crystal oscillator output impedance (Ro) and the serial resistance (Rs) is equivalent to the output line impedance (Z0).

It is possible to conduct tests to determine the optimal value for serial resistance. The testing method involves measuring with the output waveform with an oscilloscope and transitioning from low to high values for the serial resistance. The optimal resistance value is the value at which overshoot, undershoot, and ringing have all been eliminated.

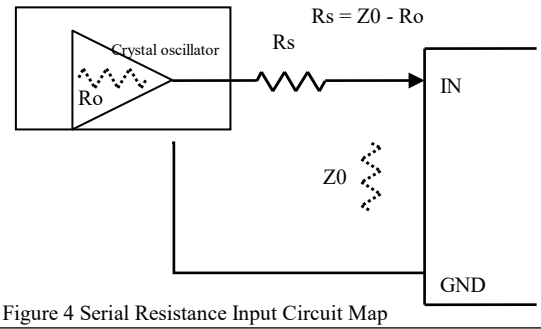
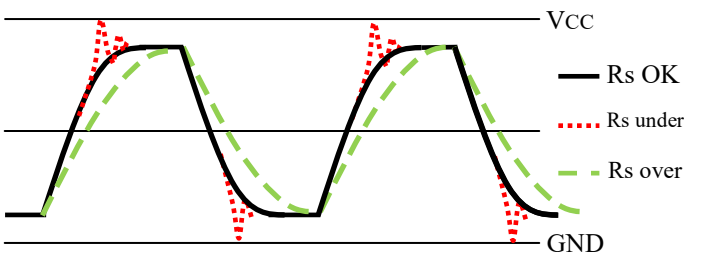



Figure 4 Serial Resistance Input Circuit Map



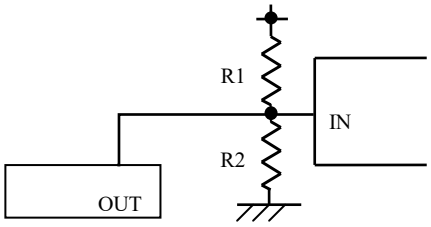

Effect on output waveform

b. Configuring termination resistance

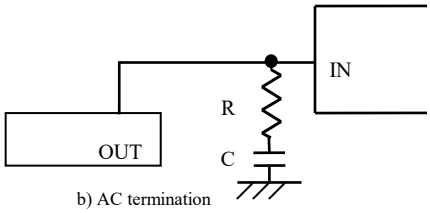
The configuration of termination resistance depends greatly on the type of interface and the type of clock line being used. Configurations will vary based on these factors.

Generally, the output waveform will experience distortion when there is a mismatch between impedance on the output line and the impedance of the device input. When impedance does not match, the traveling wave cannot be fully received, and part of the signal is reflected back towards the oscillator to cause distortion in the output waveform. This results in high-frequency noise. When branching crystal oscillator output to multiple devices, this waveform distortion can cause trigger errors. As such, proper termination and impedance matching is vital.

To prevent echoing from the receiving device, the input should be terminated with the same value as impedance on the output line. Figure 5 shows two common termination methods: split termination and AC termination.




a) Split termination




b) AC termination

Figure 5 Termination Resistance Configuration Methods

c. Filter configuration

Normally, output waveform distortion can be addressed using serial resistance or termination resistance. Filtering is used in cases where these methods do not resolve the problem. The use of a filter is an effective method for eliminating high-frequency noise, but this method will result in an increase in $t_r$ and $t_f$ (waveform dissipation). As such, you must select a filter that is appropriate for the properties of $t_r$ and $t_f$. Also, using a larger capacitor as a filter can cause an increase in electrical current flow, which can conversely result in an increase in noise.

d. Output line impedance matching

Reducing waveform echoes on the output line requires that the output line impedance be made as consistent as possible. As indicated in Figure 6, achieving consistent output line impedance involves configuring the output line pattern curve so that right angles are converted into a 45º angle or, if possible, a rounded curve. Also, avoid the use of a through-hole or a T-branch.

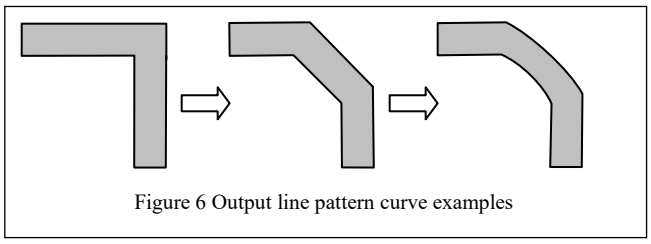


Figure 6 Output line pattern curve examples

Finally, we will introduce the two most vital methods for reducing noise emission.

a. Use a shorter output line

Among all circuits, the output line most easily produces noise. Therefore, during design and layout, high priority should be placed on allowing the shortest output line with no impedance fluctuations. The use of shorter wiring will shift the output line resonant frequency to the high frequency side. The higher the frequency, the more damping occurs on output frequency elements, which in turn results in reduced noise emission.

b. Use a shorter current loop path

As noted above, the level of noise emitted from the output line is proportionate to the current loop path length. Therefore, it is important that the output and ground traces for the crystal oscillator and input devices be made as short as possible. An easy way to achieve this is to mount the ground plane on the opposite side of the output trace.

As detailed above, careful circuit design for the crystal oscillator and its peripheral circuits is critical to noise reduction. Optimal circuit design allows the avoidance of noise-related issues and enables devices to achieve their full performance potential.

[3] Crystal units peripheral circuits

1) Crystal units and peripheral circuit mounting surface

Please lay out crystal unit, capacitors, and resistors near IC as much as possible.
Keep the wiring as short as possible and do not cross it with other signal lines.
As shown in Figure 7, it is recommended to provide a wide GND area on the same board surface where the crystal units are mounted.
Resistors Rd and Rf are omitted in Figure 7.

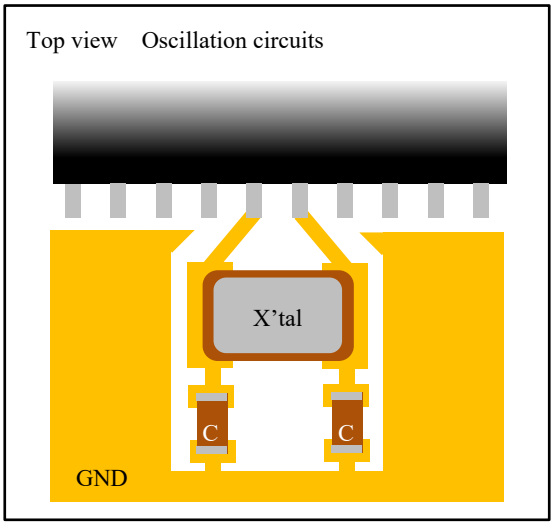



Figure 7. Crystal unit and peripheral circuits

2) Cross-section of multi-layered board

As shown in Figure 8, In case of multi-layered PCB board, do not lay out other signal lines under crystal units.
If shielding with GND is required, shield the surface farthest from the oscillation circuits.

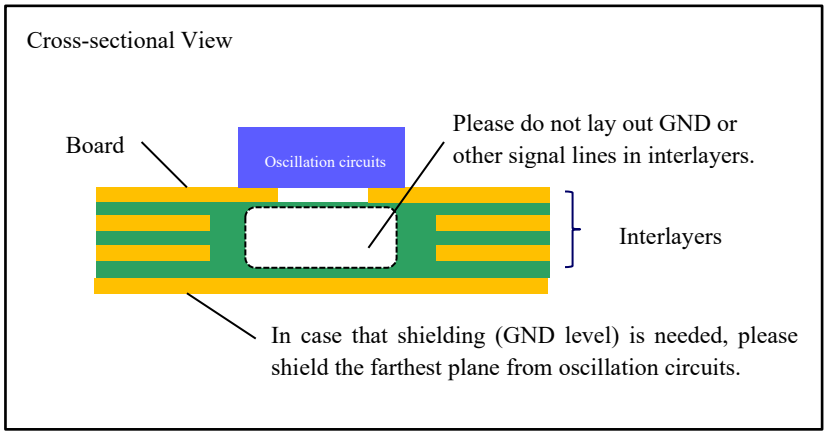



Figure 8. Cross-section of multi-layered board

[4]. At the end

Please note that the contents described here are reference examples of peripheral circuits design for crystal oscillators and crystal units, are not guaranteed.
In the case of crystal units, we recommend that you also refer to the design guides of the oscillation circuit manufacturer.