Differential Clock Drivers and Terminations

OUT-23-1737

1. Introduction

Differential clocks are widely used to achieve high-speed, noise-tolerant clock transmission. Clock manufacturers including Epson offer differential clock products in a variety of formats, and it is necessary to make the appropriate selection according to the requirements of the system. Epson has offered differential clock products in three standard formats: LV-PECL, LVDS, and HCSL, and now we have newly added our proprietary Wide-Amplitude LVDS, or WA-LVDS, to the lineup. This technical note explains the characteristics of these four differential clocks.

2. Overview of differential clocks

① LV-PECL

LV-PECL stands for “Low Voltage Positive Emitter Coupled Logic”. As you can see from the word "Emitter", it is an output driver composed of bipolar transistors. Since ECL which is a root of LV-PECL required a negative power supply, the word "Positive" was added to emphasize that the driver operates with a positive power supply. The word “Low Voltage” is further added after a product which operates with a power supply voltage of 3.3 V came out. Nowadays, since products operable with 3.3 V or lower became quite general, "LV-" is often omitted.

LV-PECL is suitable for high-speed operation because the output transistors operate without being shut off, as explained later. In addition, since the amplitude is relatively large, low phase noise feature is available, as well as excellent noise immunity.

② LVDS

LVDS stands for “Low Voltage Differential Signaling”. As the name suggests, LVDS is characterized by its low amplitude operation. LVDS was first developed mainly by National Semiconductor (later acquired by Texas Instruments). It was then standardized by ANSI/TIA/EIA in 1994 and is currently used in quite many electronic devices.

The most general amplitude level is 0.35 V (Typ.). By keeping the amplitude low, high-speed operation with low driver current is achieved. Low current consumption is a major advantage of LVDS. However, due to the low amplitude, its phase noise tends to deteriorate. In addition, it must be noted that the receiver needs a considerable amount of power to expand the amplitude to the desired level, and phase noise might be degraded during this process.

③ HCSL

HCSL stands for "High-speed Current Steering Logic". This name comes from the circuit structure that the current output path is steered alternately between positive and negative output terminals. This method was proposed in the PCI-Express standard, and it is still a major application today. The output waveform of the HCSL driver provided by Epson is adjusted so that the edged rate is appropriate or not too steep. This is because the clock frequency used for PCI-Express is 100 MHz in usual, and the edge rate is required to be fitted for that frequency. Therefore, although the amplitude level is almost the same as LV-PECL, the phase noise is somewhat disadvantageous compared to it.

④ WA-LVDS

In recent years, clock receivers on ASICs and SOCs have become more customized, so the standard differential clocks mentioned above are not always suitable. Therefore, Epson recently released Wide-Amplitude LVDS, or WA-LVDS, to provide a differential clock that provides superior performance and flexibility.

WA-LVDS maintains the simplicity of the LVDS load connection, and provides flexibility to the offset voltage and signal amplitude. The offset voltage level and amplitude can be selected from four levels and ten levels, respectively (details will be described later). Therefore, in many cases, you can connect the clock directly to your LSI without the need for extra components. Of course, AC coupling with capacitors is also possible. If you choose large amplitude, current consumption increases but lower phase noise is expected. WA-LVDS is applicable for both systems which are oriented in low consumption and low noise. Another advantage of WA-LVDS is that it has higher PSNR (Power Supply Noise Rejection) performance than LVDS.

3. Classification of differential clocks

Although it is not well recognized widely, differential clocks are broadly divided into two types: current output type and voltage output type. The current output type obtains the desired output amplitude by passing a specified current through the load resistor. Thus, the amplitude also depends on the accuracy of the load resistance. On the other hand, the voltage output type directly outputs a specified voltage to the load. The amplitude is not very dependent on the accuracy of the load resistance.

Furthermore, when classified from the perspective of the current flowing through the load resistance, the current can be divided into two types: pure AC and AC + DC. Inevitably, clock drivers that include a DC component require an excess current consumption.

Based on these combinations, differential clocks can be classified into four types which are shown in Table 1. The newly developed WA-LVDS is a voltage output type, and the current flowing through the load resistance is pure AC. This is exactly an ideal combination for a differential clock.

Table 1. Classification of differential clocks

	Voltage Output Type	Current Output Type
Pure AC	WA-LVDS	LVDS
AC + DC	LV-PECL	HCSL

Note 1: Some products have a pseudo-realization of LV-PECL as a current output type.

Note 2: LP-HCSL (Low-Power HCSL) which is proprietary to Renesas (formerly IDT) is a kind of HCSL, but it belongs to the same classification as LV-PECL.

4. Output voltage and current

Let's look at the differences in output voltage for the three existing clocks, i.e., LV-PECL, LVDS, HCSL. Please refer to Figure 1.

The most unique one may be LV-PECL. The output voltage of LV-PECL is defined with respect to the supply voltage V_{CC}. Therefore, the output voltage value changes depending on the supply voltage. Specifications of the H level output voltage V_{OH} and L level output voltage V_{OL} are shown in the figure. The differential amplitude is 0.7625 V (Typ.) regardless of V_{CC}.

For LVDS, the offset voltage V_{OS} is specified as 1.25 V and is independent of the supply voltage. The differential amplitude V_{OD} is 0.35 V, which is significantly the smallest value among the three methods.

The last one, HCSL is characterized by the L level being 0 V. The specification usually determines a differential crossing point voltage V_{CR} of 0.4 V. There are often no clear regulations regarding the H level. But inevitably, it is designed around 0.8 V. Hence, the amplitude level is approximately the same as LV-PECL.

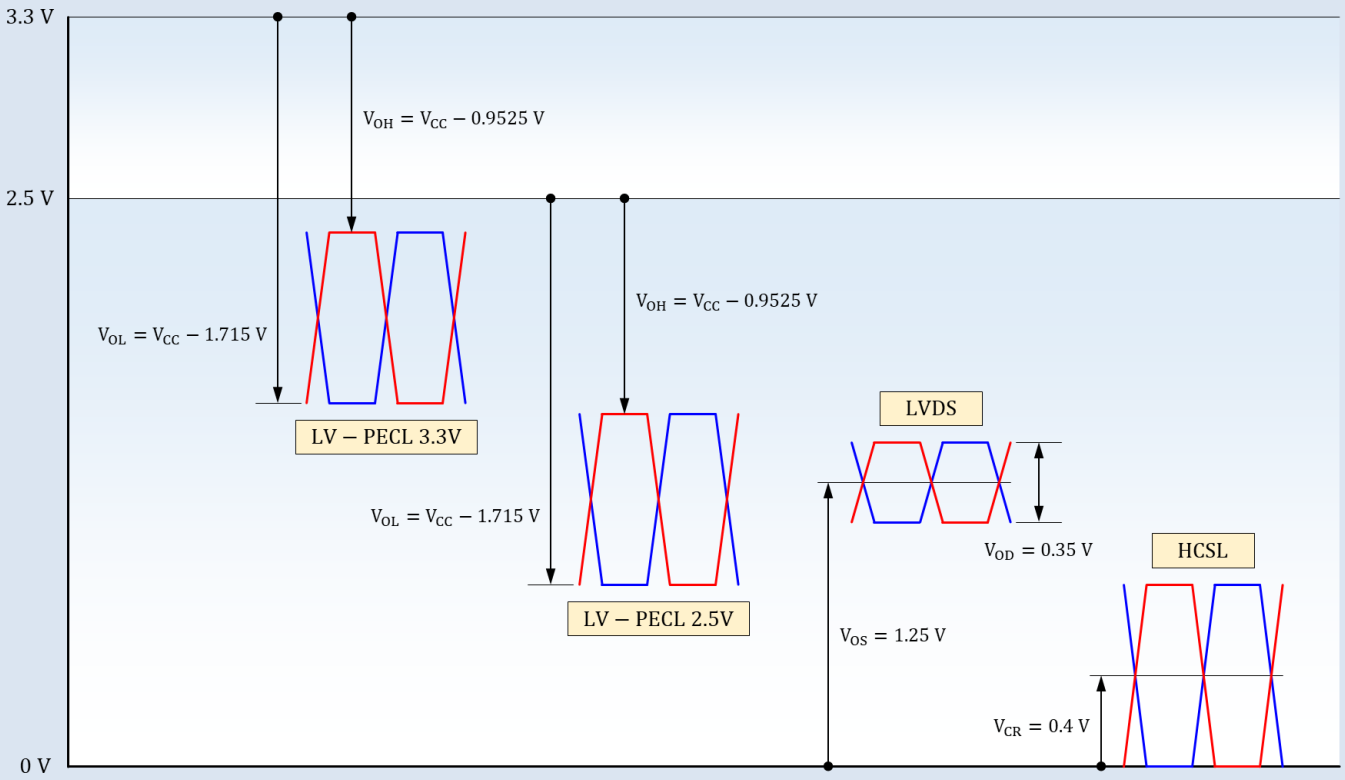

Figure 1. Differential clock output voltage comparison

Next, let's look at the output current. The output current here means the current that flows from the driver's output terminals to the load (or flows in from the load) which forms the output voltage indicated in Figure 1. Please refer to Figure 2.

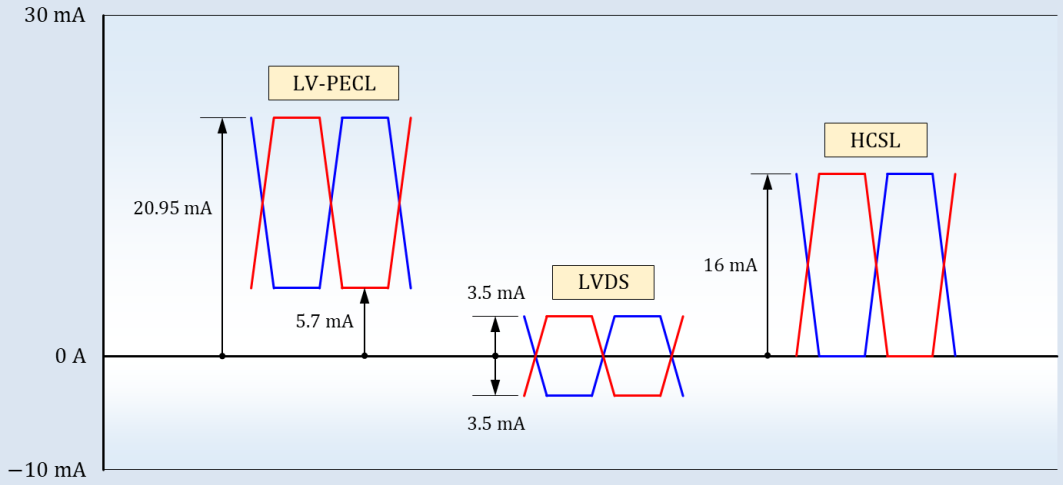

Figure 2. Differential clock output current comparison

As mentioned, the output voltage of LV-PECL depends on the supply voltage, but the output current is independent of supply voltage. This is because the termination reference voltage also varies according to the supply voltage. LV-PECL driver is required to provide 5.7 mA even when outputting L level. This is a major disadvantage of LV-PECL in terms of current consumption.

What makes LVDS unique is that the output current is pure AC, so no excess current is required. Further, since the peak output current is limited to small value of 3.5 mA, LVDS is suitable for low power applications. LVDS's pure AC current output also enables AC coupling the clock signal with a capacitor.

HCSL outputs no current when outputting L level. Therefore, even though the output voltage amplitude is comparable to LV-PECL, the output current is much lower.

5. Circuit operation and termination method

Next, let us explain in detail the circuit operation of each type and how to connect the load.

① LV-PECL

A typical termination method for LV-PECL is shown in Figure 3. It is specified that the 50 Ω termination must be done to V_{CC} – 2 V, not to ground. Since the potential V_{CC} – 2 V must be created by the user, the clock receiving circuit would be somewhat complex.

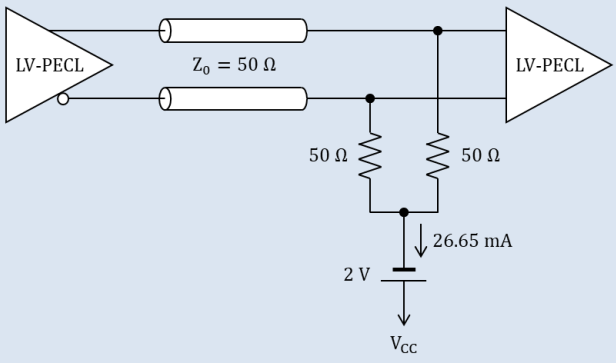

Figure 3. LV-PECL termination

The currents flowing through the loads on the H and L level output, which are shown in Figure 2, are respectively calculated as follows.

$$I_{OH} = \frac{V_{CC} - 0.9525\ \text{V} - (V_{CC} - 2\ \text{V})}{50\ \Omega} = 20.95\ \text{mA}$$

$$I_{OL} = \frac{V_{CC} - 1.715\ \text{V} - (V_{CC} - 2\ \text{V})}{50\ \Omega} = 5.7\ \text{mA}$$

From the above formula, it can be understood that a total of 26.65 mA of current is output from output terminals.

It is not practical to provide a constant voltage source of V_{CC} – 2 V only for this termination. Thus, an alternative method is usually adopted. Figure 4 shows what is called Y-bias termination, a method in which a current of 26.65 mA flows through a resistor to create a voltage equivalent to V_{CC} – 2 V. The resistance value R_T must be set according to V_{CC} as noted in the figure. If V_{CC} = 3.3 V, R_T = 49 Ω; or if V_{CC} = 2.5 V, R_T = 19 Ω. A capacitor may be connected in parallel with R_T to let the termination node more ideal as an AC ground.

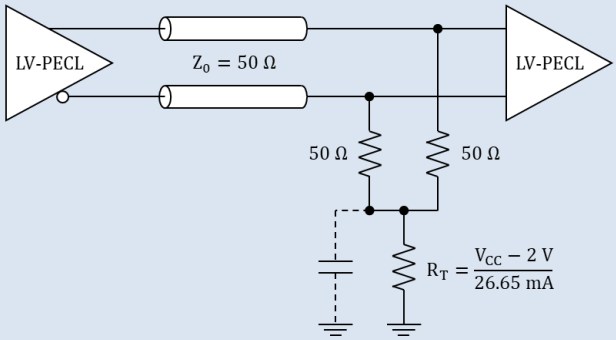

Figure 4. LV-PECL termination（Y-bias termination）

Figure 5 shows another method. The resistor R_T is divided into two equivalent resistors ($2R_T$), and each is integrated with a load resistor (50 Ω), thereby reducing the need for only two resistors. The resistance value is 148 Ω if V_{CC} = 3.3 V, and 88 Ω if V_{CC} = 2.5 V. The total output current will be the same as Figure 4, but the current value flowing from each output terminal is different, and this will cause a slight deviation in the voltage value. Also, since the circuit is not terminated to AC ground with 50 Ω, this termination cannot be applied at the end of the transmission line. It can be applicable only when the clock driver and the receiver circuit are placed in proximity. In addition, please note that Epson does not guarantee the clock characteristics using this termination method.

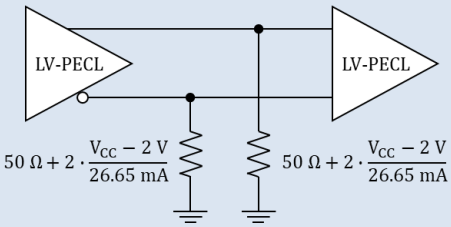

Figure 5. LV-PECL termination (Simple method)

Finally, we will introduce a technique called Thevenin termination. This requires four resistors but is the most straightforward. As shown in the left diagram of Figure 6, consider that the voltage V_{CC} is divided by two resistors R_1 and R_2 and the midpoint node is taken out. If we transform this circuit using Thevenin's theorem, we will obtain the equivalent circuit on the right. It can be seen that V_{CC} – 2 V and 50 Ω are equivalently created at the node. Applying this circuit to the load circuit in Figure 3 results in the termination shown in Figure 7. This is so-called the Thevenin termination. When you use this technique, the output impedance of the V_{CC} supply must be kept sufficiently low relative to the value of R_1. Additionally, you need to be careful about the noise in V_{CC}, since it may degrade the clock quality.

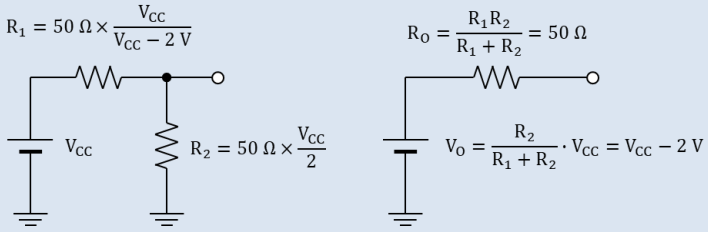

Figure 6. Equivalent termination based on Thevenin's theorem

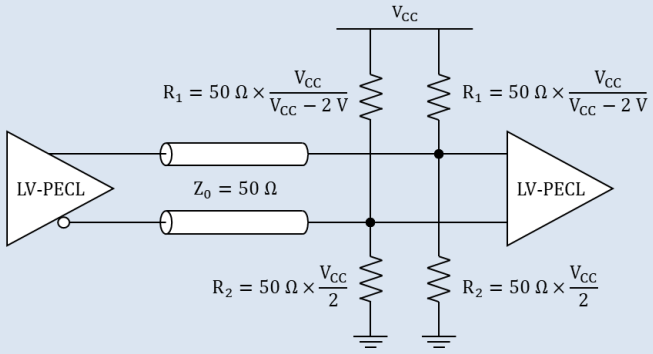

Figure 7. LV-PECL termination (Thevenin's method)

Next, let's examine the internal circuit configuration of the LV-PECL driver shown in Figure 8. The output stage is an open emitter configuration with a common collector. This is a circuit generally called an "emitter follower" since the emitter potential changes following the base potential. By switching the constant current "I" with a MOS transistors, either V_{CC} or V_{CC} – 0.8 V is alternately applied to the base terminals of the bipolar transistors.

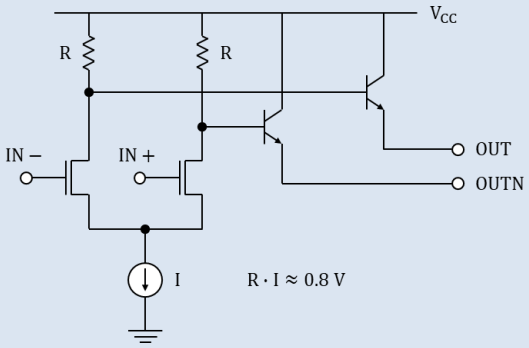

Figure 8. LV-PECL driver circuit

Figure 9 demonstrates how the output voltage and current of LV-PECL are determined. The current I_{BJT} through the bipolar transistor and the current I_L through the load resistor are expressed using output voltage V_{OUT} as a parameter. The output voltage and current are determined at the point where those two balance each other.

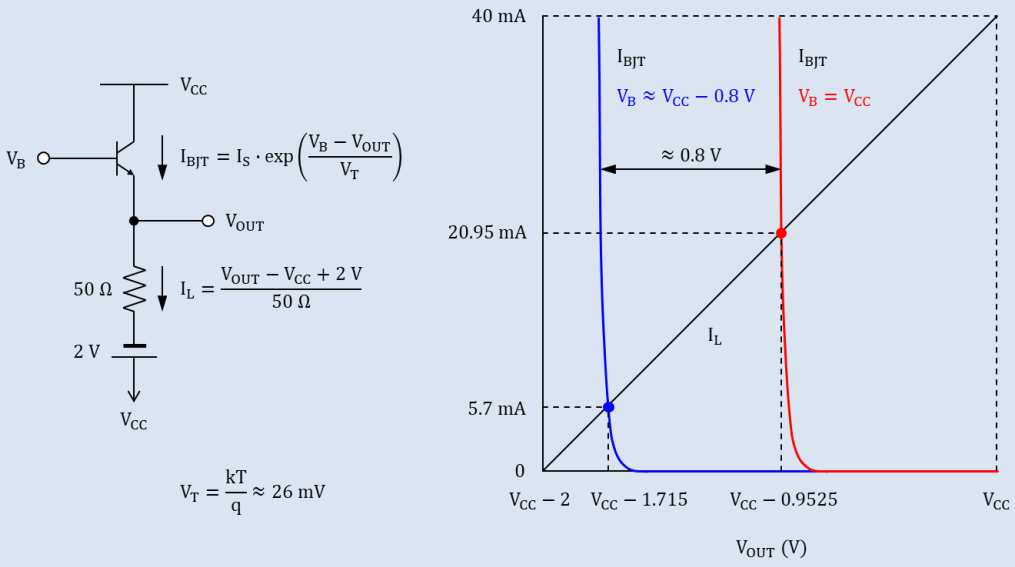

Figure 9. Determination of the LV-PECL output voltage and current

If the base voltage V_B is equal to V_{CC}, the I_{BJT} will be the red line on the graph. I_{BJT} and I_L must balance when V_{OUT} is V_{CC} – 0.9525 V and the current value at that point must be 20.95 mA in accordance with the LV-PECL specifications. To satisfy such characteristics, the size of the bipolar transistor is adjusted. When the base voltage of this transistor is lowered to V_{CC} – 0.8 V, the I_{BJT} follows a blue line. Under this condition, I_{BJT} and I_L are balanced when V_{OUT} is V_{CC} – 1.715 V, and the current value at this point is 5.7 mA. In this way, the L level specification of LV-PECL is satisfied.

If the load resistance deviates from 50 Ω, the slope of the I_L plot (black line) will increase or decrease. However, you can understand that even in that case, the amount of change in the output voltage is small. From this feature, it can be said that LV-PECL is a voltage output type driver. Note that recent Epson's LV-PECL drivers use MOS transistors instead of bipolar transistors. In this case, a unique circuit configuration slightly different from that in Figure 8 is implemented, but its explanation will be omitted here.

By the way, you may find it strange that V_{OH} and V_{OL} are specified as quite detailed numbers with 3 to 4 digits after the decimal point. This is probably because the specifications were set to mimic the characteristics of the product that first released. In actual, these numbers differ slightly depending on the manufacturer and product, so please check data sheets when you choose a product.

Some LV-PECL drivers use a current output type circuit as shown in Figure 10. The same results as the voltage type can be obtained if the load is 50 Ω, but the simple termination method shown in Figure 5 cannot be applied for this type of drivers. A demerit of this circuit is that it tends to be more susceptible to parasitic inductance compared to emitter follower circuits. Thus, ringing may be superimposed on the clock waveform. Epson used to use this kind of circuit in some of SAW oscillators, but now all the LV-PECL are unified to voltage output type.

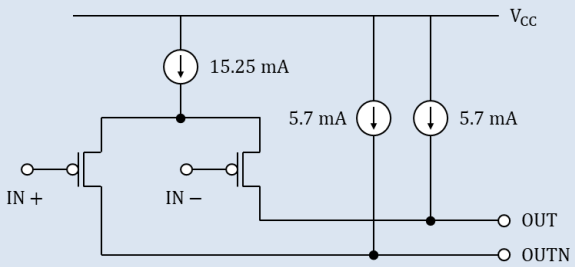

Figure 10. Current output type pseudo LV-PECL driver

② LVDS

The LVDS termination methods are shown in Figure 11. Since the output current of LVDS is pure AC, the 50 Ω load is connected to a floating node as shown in the left diagram. This node is constant at 1.25 V, thus it is considered to be an AC ground. The 1.25 V voltage is set by the driver, so there is no need to provide a bias voltage on the receiver side. You can also connect a capacitor at the terminating node to let the AC ground more ideal. This may be also effective to eliminate common mode noise. But in usual, it is not necessary. In many cases, the two 50 Ω resistors can be replaced with one 100 Ω resistor to create a differential 100 Ω termination, as shown in the right figure.

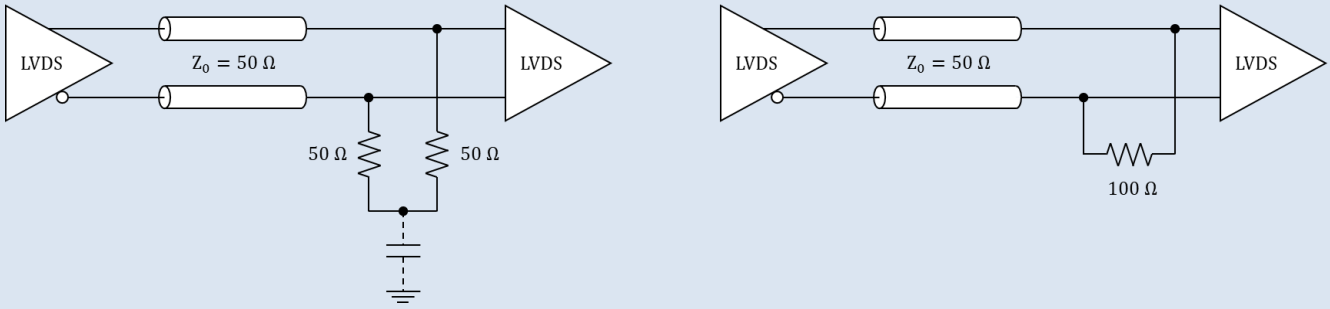

Figure 11. LVDS Terminations

Since the output current of LVDS is pure AC, it can be used with AC coupling capacitor as shown in Figure 12. The capacitor can be inserted at either the transmitting side or receiving side of the transmission line. In this case, you need to prepare a bias voltage V_b on the receiving side. The value of V_b can be set arbitrarily according to the specifications of the receiving circuit. V_b needs to be a sufficiently low impedance voltage source to warrant a 50 Ω termination, or conversely, a sufficiently high impedance to warrant a differential 100 Ω termination. You can also use the Thevenin termination shown in Figure 7.

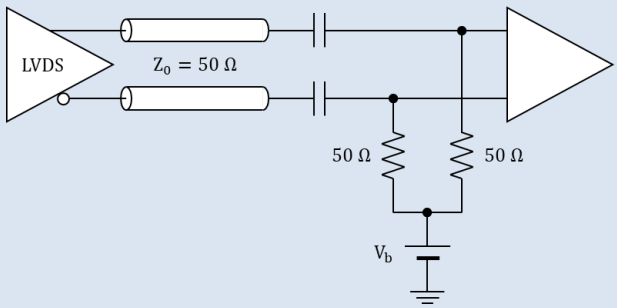

Figure 12. LVDS Termination（AC Coupled）

Note that if the clock duty ratio deviates from 50 %, a DC component will appear in the output current. In this case, charge may accumulate in the AC coupling capacitor, causing changes in the waveform. The degree of change depends on the product's circuit design, so please check carefully before using.

Figure 13 shows the internal circuit configuration of the LVDS driver. It consists of a constant current source of 3.5 mA, four MOS switches, and a variable resistor using active elements. The center and right figures in Figure 13 show the switching operation of the current path. By alternating between these two states, AC current flows through the load.

Constant current of 3.5 mA always flows through the resistor, so offset voltage V_{OS} can be adjusted by changing its resistance. LVDS drivers have CMFB (Common Mode Feedback) circuits that functions to keep V_{OS} at 1.25 V. There are three types of CMFB circuits: one that monitors the actual output waveforms, one that estimates V_{OS} from a replica of the driver circuit inside the IC, and a hybrid type of both.

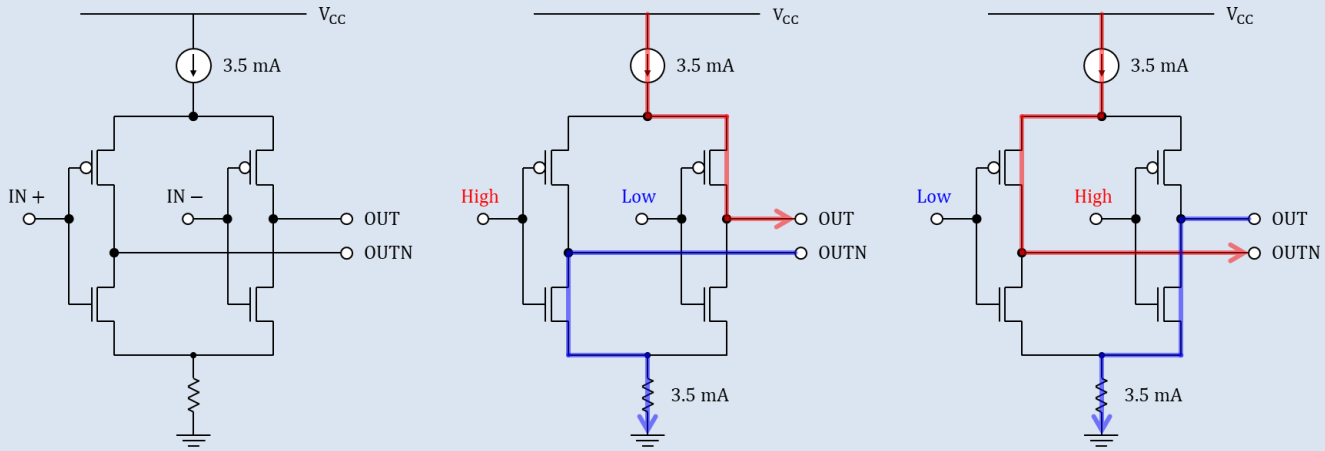

Figure 13. LVDS Driver Circuit

③ HCSL

The HCSL termination methods are shown in Figure 14. The left side of the figure shows an example of termination on the receiving side. This is a simple, easy to understand, and less problematic termination method. The load on the high-level output side is supplied with a current of 16 mA from the HCSL driver, generating an amplitude of 0.8 V. The current supply to the load on the low-level output side is shut off and the voltage becomes ground level.

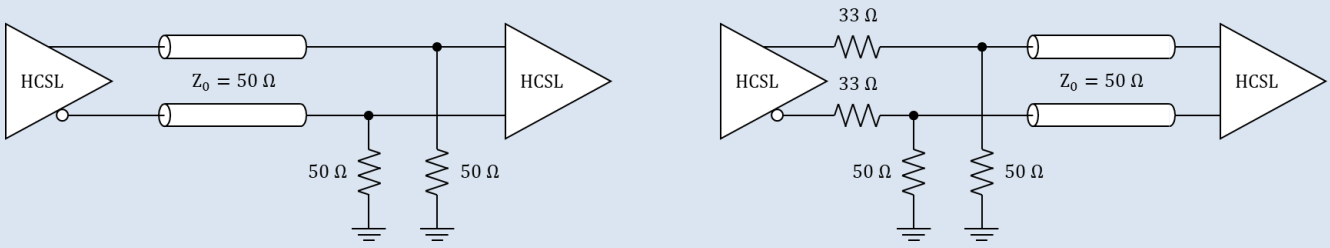

Figure 14. HCSL Terminations

Another termination method as shown in the right side of Figure 14 is specified in the PCI-Express standard. Terminating resistors are provided on the driver side, and the current output from the driver is divided into two directions: into the 50 Ω load and the receiving circuit. At the receiver terminal, the waveform is totally reflected, hence the amplitude is doubled, and a waveform with 0.8 V amplitude is formed. The reflected waveform is absorbed by 50 Ω, but because the HCSL driver is connected, the impedance is slightly lower than 50 Ω. To let the driver less visible from the nodes, 33 Ω resistors are inserted at the output terminals of the driver. However, even with this approach, it is difficult to ensure perfect impedance matching. Thus, some waveforms will be re-reflected at the driver side. Therefore, the waveform at the receiver terminals changes depending on the electrical length of the transmission line. You must design your circuit with this behavior in mind. Waveforms can be simulated using IBIS models provided by clock manufacturers.

Terminations in Figure 14 are based on differential 100 Ω transmission, but differential 85 Ω may also be used. The purpose of this is to reduce the size of the circuit board by narrowing the spacing between transmission lines, or to reduce the thickness of the board. In this case, resistances must be 42.5 Ω instead of 50 Ω, and 27 Ω instead of 33 Ω. As the voltage amplitude must be kept, (100/85) times the output current is required.

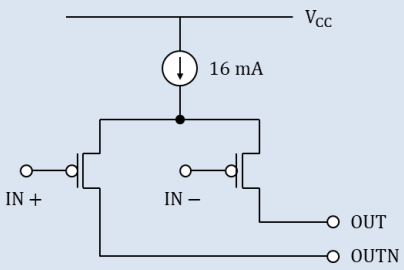

Figure 15. HCSL Driver Circuit

Figure 15 shows the internal circuit configuration of the HCSL driver. It has a simple configuration in which a constant current of 16 mA is alternately applied to two output terminals with MOS switches. This circuit is very similar to the circuit in Figure 10, with the useless 5.7 mA constant current sources removed.

The AC impedance of the constant current source is ideally ∞, and the AC impedance of the MOS switches is ideally 0 (in the on state) or ∞ (in the off state), so even in the case of the connection shown on the right in Figure 14, the HCSL driver basically won't be a cause of impedance mismatch. However, there are factors such as parasitic capacitance that disrupt the ideal state, so impedance mismatch is unavoidable in actual.

④ WA-LVDS

The WA-LVDS termination method is the same as LVDS, so please refer to Figure 11 or 12. In the case of LVDS with an AC-coupled load, if the duty ratio deviates from 50 %, a DC current will arise, and there is a concern that charge will accumulate in the capacitor. Since WA-LVDS is a voltage output type, the advantage is that there are fewer such concerns.

With LVDS, the offset voltage (V_{OS}) is fixed at 1.25 V and the differential output voltage (V_{OD}) is fixed at 0.35 V, but with WA-LVDS, you can select from 4 levels and 5 levels, respectively, as shown in the tables below. The selectable values depend on the power supply voltage V_{CC}. When AC-coupling, select a V_{OS} value close to $V_{CC}/2$.

Table 2. V_{OS} selection of WA-LVDS

V_{OS}	V_{CC}		
	1.8 V	2.5 V	3.3 V
1.65 V	–	–	○
1.5 V	–	–	○
1.25 V	–	○	○
0.9 V	○	○	○

Table 3. V_{OD} selection of WA-LVDS

V_{OD}	V_{CC}		
	1.8 V	2.5 V	3.3 V
0.8 V	–	○	○
0.05 V Step	–	○	○
0.4 V	–	○	○
0.35 V	○	○	○

Figure 16 shows the internal circuit configuration of the WA-LVDS driver. N-type MOS transistors are connected to the V_{CC} side, P-type MOS transistors are connected to the ground side, and the source terminals are connected to the output. This is a configuration called a source follower circuit which is like the emitter follower circuit of the LV-PECL. The output voltage level depends on the potentials of IN+ and IN– which are input to the gate terminals. A unique circuit is implemented to control the input amplitude potential to satisfy desired V_{OS} and V_{OD}. The current path switching operation is shown in the center and right figures of Figure 16. Its behavior is like that of LVDS.

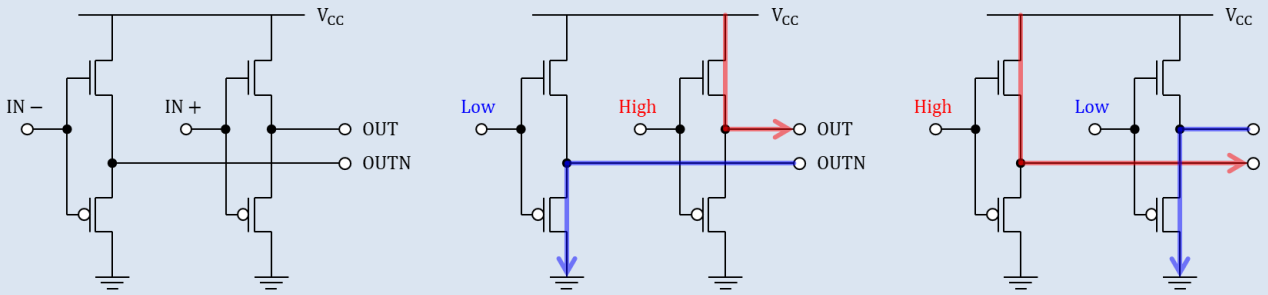

Figure 16. WA-LVDS Driver Circuit

Referring to Figure 17, let's see how the WA-LVDS output voltage and current are determined. They are determined by the balance between the current I_{DN} flowing through the N-type MOS transistor, the current I_L flowing through the 100 Ω load resistance, and the current I_{DP} flowing through the P-type MOS transistor.

The graph in Figure 17 shows a state in which a waveform of V_{OS} = 1.25 V and V_{OD} = 0.8 V is output. I_{DN} and I_{DP} are determined by the gate-source voltage of each MOS transistor. All current values change when the source voltage changes. Assume V_{SN} and V_{SP} which will flow the same current of I_{DN} and I_{DP} (8 mA in the figure). If the difference between V_{SN} and V_{SP} is 100 times the current value (0.8 V in the figure), then I_L will also have the same current value and the circuit will be in equilibrium.

By appropriately adjusting the gate voltages of the MOS transistors V_{GN} and V_{GP}, the above equilibrium point can be set arbitrarily, making it possible to satisfy the desired offset voltage V_{OS} and differential output voltage V_{OD}. An internal adjustment mechanism for this purpose is implemented in the WA-LVDS driver IC.

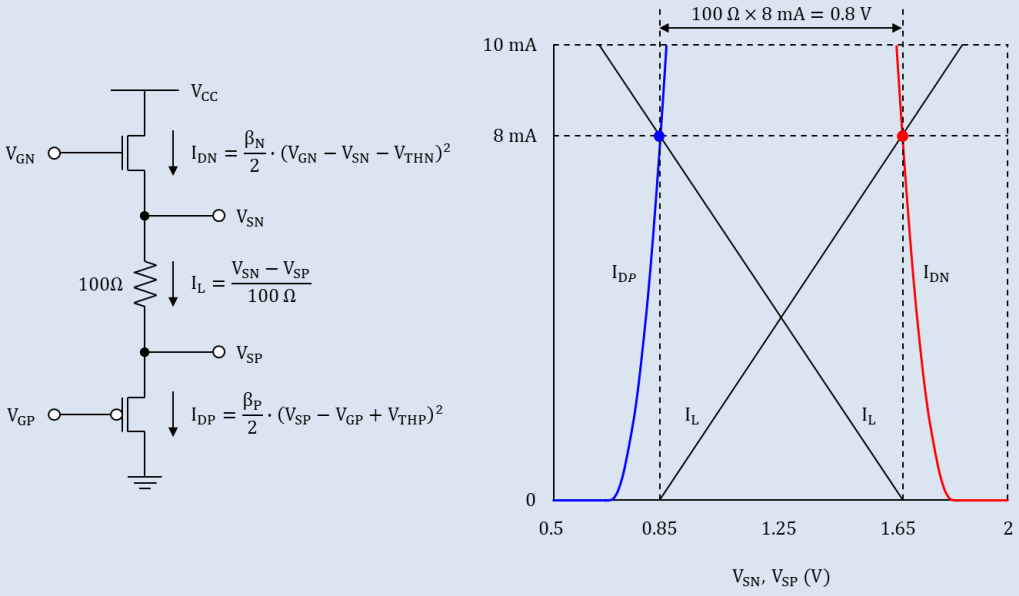

Figure 17. Determination of the WA-LVDS output voltage and current

6. Correlation between output amplitude, output current and jitter

Let's compare the correlation between output amplitude and output current for the four methods mentioned above. Please see Figure 18.

WA-LVDS (blue ●) has 10 plots because the differential output voltage V_{OD} can be switched in 10 steps. The waveform formation method is the same as LVDS, so when V_{OD} is 0.35 V, it matches LVDS. The current increases each time the amplitude is increased, but the output current remains at 8 mA even when V_{OD} is 0.8 V. This is because the output current is pure AC.

In contrast, HCSL requires twice as much, 16 mA, even though the amplitude is the same at 0.8 V. LV-PECL requires a current of 26.65 mA even though its amplitude is slightly smaller. By comparing like this, you can see how efficient WA-LVDS is.

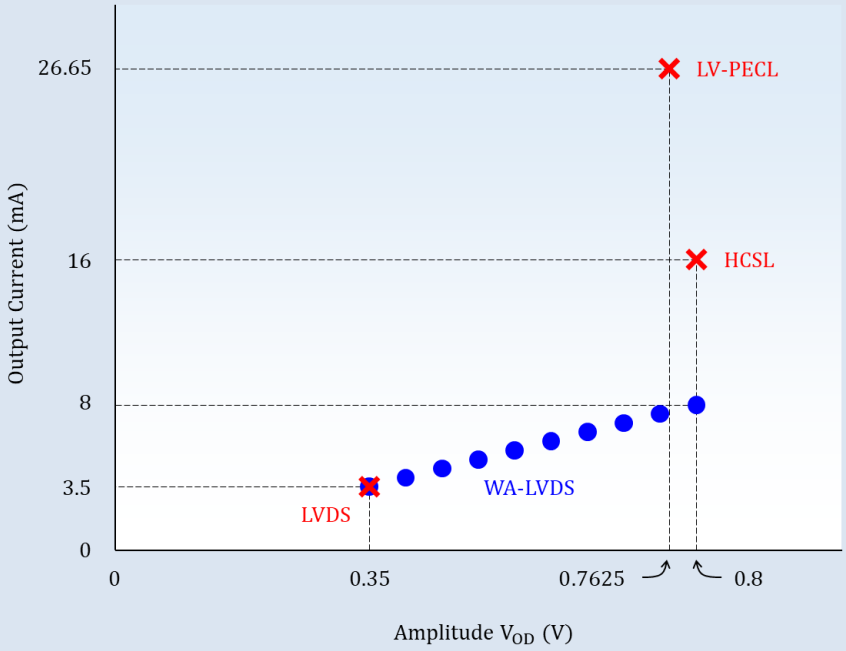

Figure 18. Correlation between output amplitude and output current of each method

An example of measured phase jitter of WA-LVDS is shown in Figure 19. It is clearly seen that the phase jitter decreases as the differential amplitude V_{OD} increases. Therefore, if the current consumption of your circuit is not constrained, a higher differential amplitude V_{OD} is a better choice for higher circuit performance.

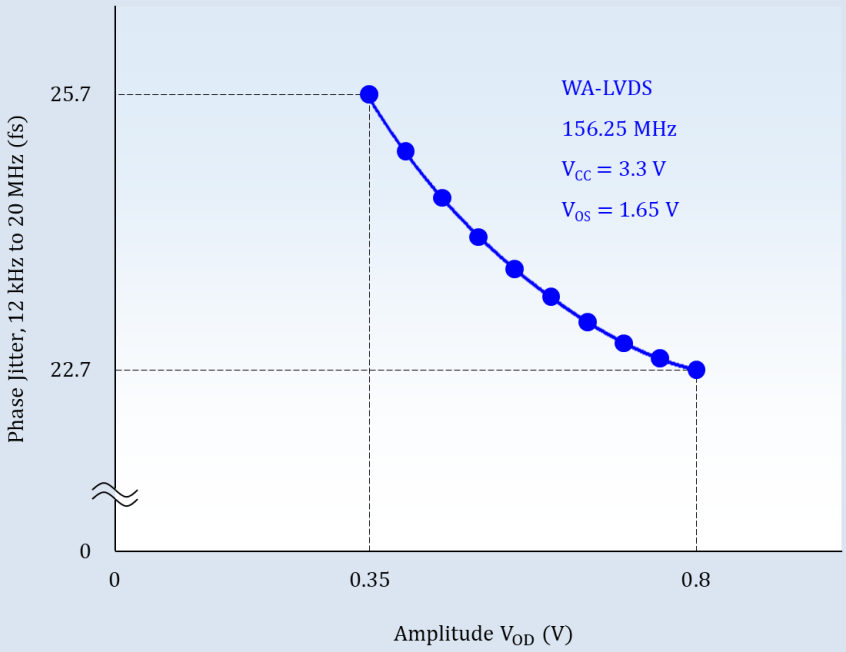

Figure 19. Phase jitter measurement example of WA-LVDS

7. Conclusion

We explained the features and usage of the three types of drivers LV-PECL, LVDS, and HCSL, as well as the newly developed WA-LVDS. Epson plans to expand WA-LVDS product lineup in the future. If you have any questions regarding the contents of this technical note, please contact us according to the information below.

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