# High-Stability Time Adjustment with Real-Time Clock Module

## An explanation of an Epson real-time clock module with sub-second time adjustment function

[**Preface**]

   In recent years, it has become simple to check the time with a very high level of accuracy. Radio clocks are common and devices can get standard time data from NTP servers. In fact, system design now assumes the ability to use accurate time data. This is necessary in many applications: banking, traffic management, power control, crime prevention, sports, and more. These systems demand accurate timing in order to synchronize multiple terminals with incoming and outgoing data. Epson offers a family of real-time clock (RTC) modules to meet this need.    Each module contains a crystal element that oscillates at a highly stable frequency.

   Every RTC module contains a crystal element and an IC with an oscillation circuit and calendar function.    Epson has improved on this basic module with the addition of a DTCXO temperature compensation function. The real-time clock modules RX-4803SA/LC and RA4803SA (both with serial interface and referred to below as the 4803 series) and RX-8803SA/LC and RA8803SA (both with $I^2C$ interface and referred to below as the 8803 series) offer improved stability and flexibility. These products can maintain frequency output stability of $\pm 3.4 \times 10^{-6}$ (a monthly error of 9 seconds) over a temperature range of -40 to +85°C. This translates into a daily error of only ±0.3 seconds.

   While these are highly accurate products, customers in certain applications need adjustment of very fine (sub-second) errors. Timekeeping devices measure time by using a 32.768 kHz crystal unit as the oscillator and dividing down to seconds. However, in applications that require synchronization of events across multiple devices, adjustment of sub-second errors is necessary (see Fig. 1). Products in the 4803 and 8803 series have a function that can adjust for sub-second errors to meet this need.

   Many Epson real-time clock modules have a RESET function, which uses software to adjust the time. This function can adjust for sub-second errors, as described above, but introduces its own small time delay due to the software's processing time. Even this error is a problem for users demanding high accuracy synchronization. The 4803 and 8803 series, therefore, have the ERST function to account for this delay through hardware.

This White paper discusses the RESET and ERST functions, which are provided in the Epson real-time clock modules with built-in DTCXO (4803 and 8803 series) and support sub-second time adjustment. It also explains how the functions work, using figures such as timing charts with specific examples of time adjustment.



Fig 1: Sub-second time adjustment in a security camera system
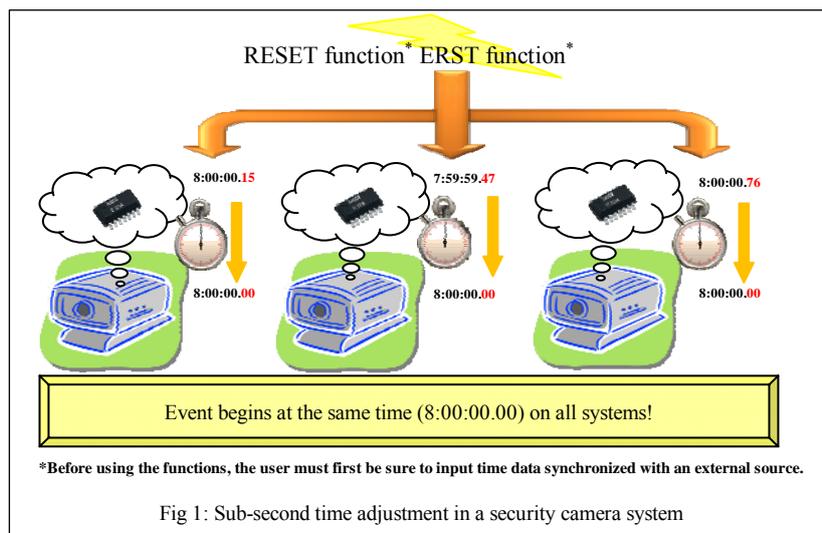
[Method of high-accurate (sub-second) time adjustment with Epson real-time clock modules]

Epson real-time clock modules (4803 and 8803 series) perform high-accuracy (sub-second) time adjustment with the two methods shown below.

1. Time adjustment with RESET bit: software-based time adjustment
2. Time adjustment with ERST bit: hardware-based time adjustment

Below is a detailed explanation of the relevant registers and examples of reset actions and settings for each method.

Before performing the above methods, the user must first be sure to input time data synchronized with an external source.

1. Example of time adjustment with RESET bit

Time adjustment with a RESET bit is a software-based method. The time can be adjusted by manipulating the real-time clock module's register. This method is used in many Epson real-time clock modules, not just the 4803 and 8803 series.

• Relevant register

● 4803 series (banks 1, 2)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| F | Control register | CSEL1 | CSEL0 | UIE | TIE | AIE | EIE | ○ | **RESET** |

● 8803 series (banks 1, 2)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0F, 1F | Control register | CSEL1 | CSEL0 | UIE | TIE | AIE | ○ | ○ | **RESET** |

• Explanation of RESET bit and its action (including timing chart example)

If the RESET bit is set to "1," the sub-second counter of the clock circuit is reset when the command ends. To ensure that clock action begins correctly at a certain time, set the desired time, then reset it. Subsequently, the seconds counter will be updated every second.
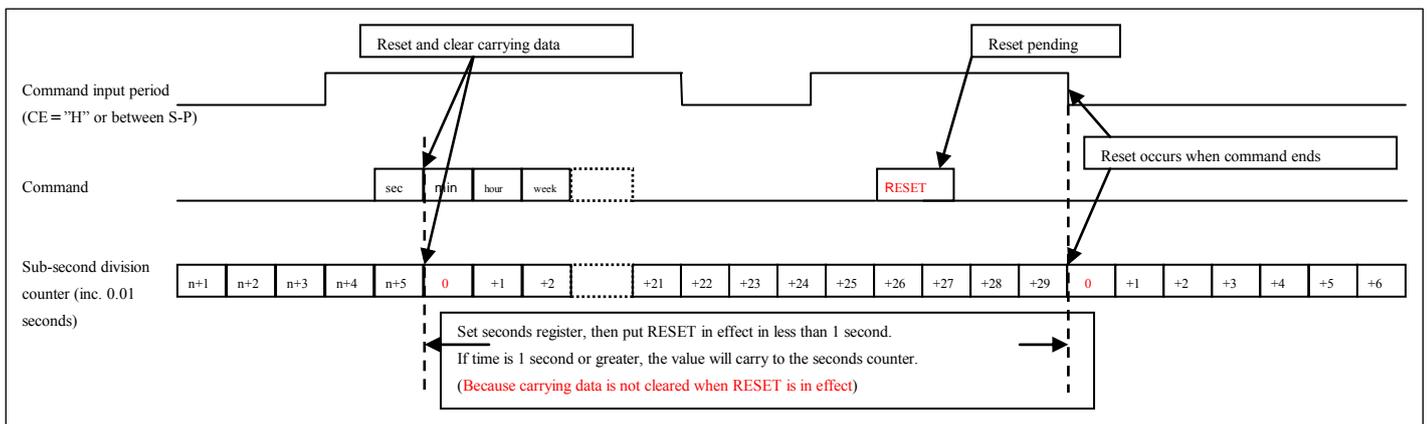


• Cautions when using RESET bit

The RESET bit action assumes the following conditions:

When the RESET bit becomes "1," that alone does not cause the counter to stop (it will continue to count).

The RESET action occurs independently from other commands. If data is written in the RESET bit, the sub-second counter will be reset when the command input period ends.

In this regard, Set the seconds register, and then reset the sub-second counter in less than 1 second, since carrying data will not be cleared when the RESET bit is in effect.

2. Example of time adjustment with ERST bit

Time adjustment with an ERST bit is a hardware-based method. The time can be adjusted by first setting the register, then inputting an event signal. Unlike time adjustment with a RESET bit as explained earlier, there is no time lag resulting from software processing time. As a result, time can be synchronized more accurately.

• Relevant register

● 4803 series (bank 3)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| F | Event control | ECP | EHL | ET1 | ET0 | ○ | ○ | ○ | **ERST** |

● 8803 series (bank 3)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| 2F | Event control | ECP | EHL | ET1 | ET0 | ○ | ○ | ○ | **ERST** |

• Explanation of ERST bit and its action (including timing chart example)

If the ERST bit is set to "1," the sub-second counter of the clock circuit is reset in synchronization with the detection of an external event input to the EVIN terminal. To ensure that clock action begins correctly at a certain time, set the time, then input an event to the EVIN terminal. Subsequently, the seconds counter will be updated every second. Event detection resulting from signal input to the EVIN terminal will be L level detection if the EHL bit is "0" and H level detection if the EHL bit is "1."[*a]

The following example shows the action that occurs when the EHL bit is set to "1" (H level detection).
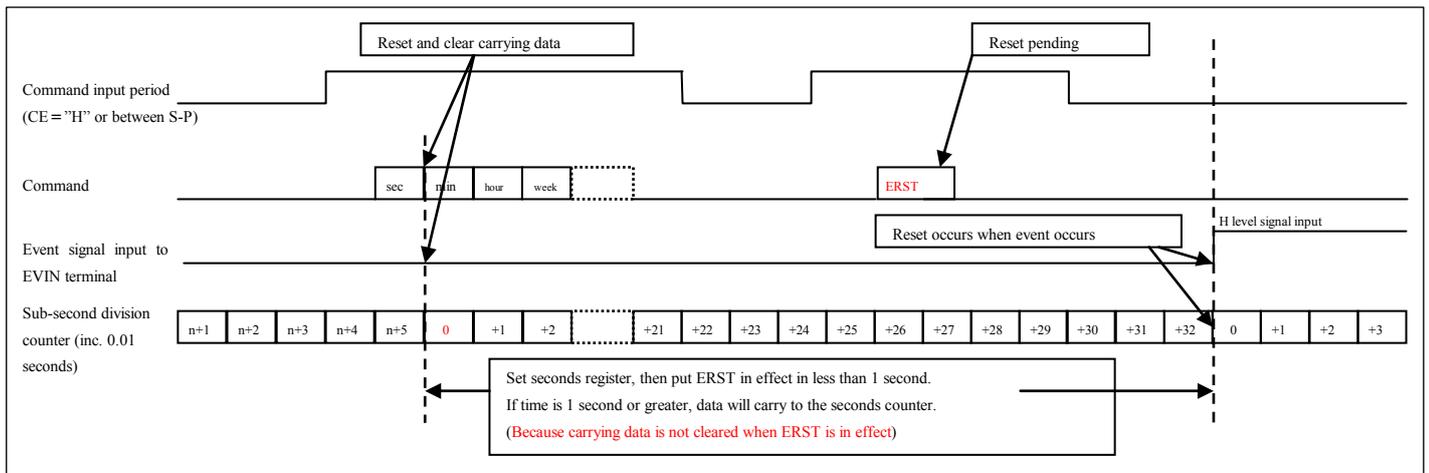


• Cautions when using ERST bit

The ERST bit action assumes the following conditions:

When the ERST bit becomes "1," that alone does not cause the counter to stop (it will continue to count).

The ERST action occurs independently from other commands. If data is written in the ERST bit, the sub-second counter will be reset when there is event input.

In this regard, Set the seconds register, and then reset the sub-second counter in less than 1 second, since carrying data will not be cleared when the ERST bit is in effect.

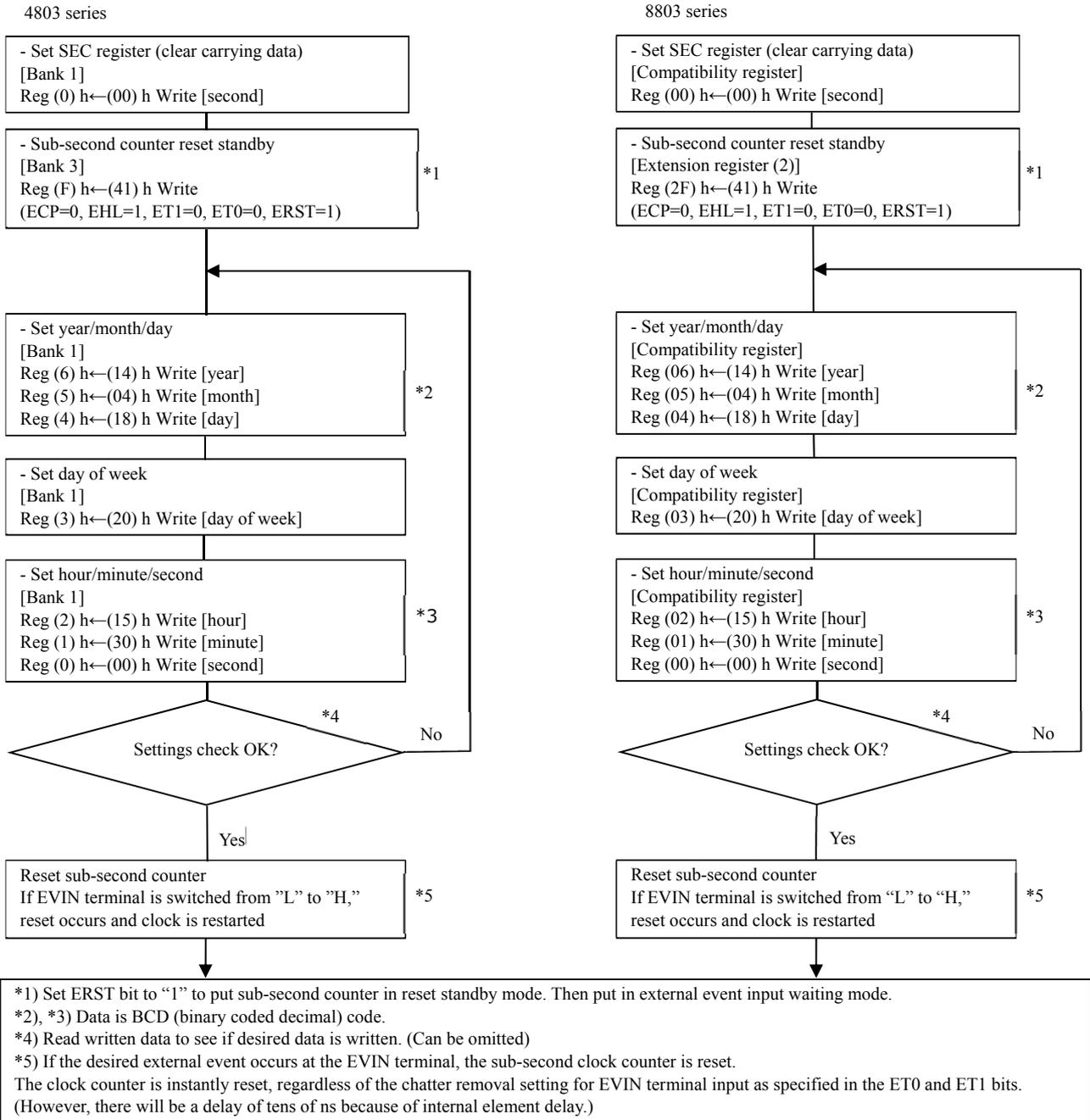After writing "1" in the ERST bit, if "0" is then written in the ERST bit before the event occurs, the ERST function will no longer be effective.

(*a)  During high-accurate time adjustment, signal detection proceeds without removing input chatter. However, because the internal clock synchronizes clock action and EVIN terminal input, it is necessary to sustain the pulse width for a minimum time of 367 µs.

• Example of setting high-accuracy time adjustment with ERST bit
  In this example, the time and calendar are being set. [Set value: Friday, April 18, 2014, 15:30:00]

**4803 series**

- Set SEC register (clear carrying data)
[Bank 1]
Reg (0) h←(00) h Write [second]

- Sub-second counter reset standby
[Bank 3]
Reg (F) h←(41) h Write
(ECP=0, EHL=1, ET1=0, ET0=0, ERST=1)     *1

- Set year/month/day
[Bank 1]
Reg (6) h←(14) h Write [year]
Reg (5) h←(04) h Write [month]
Reg (4) h←(18) h Write [day]     *2

- Set day of week
[Bank 1]
Reg (3) h←(20) h Write [day of week]

- Set hour/minute/second
[Bank 1]
Reg (2) h←(15) h Write [hour]
Reg (1) h←(30) h Write [minute]
Reg (0) h←(00) h Write [second]     *3

*4
Settings check OK?     No

Yes

Reset sub-second counter
If EVIN terminal is switched from "L" to "H,"
reset occurs and clock is restarted     *5

**8803 series**

- Set SEC register (clear carrying data)
[Compatibility register]
Reg (00) h←(00) h Write [second]

- Sub-second counter reset standby
[Extension register (2)]
Reg (2F) h←(41) h Write
(ECP=0, EHL=1, ET1=0, ET0=0, ERST=1)     *1

- Set year/month/day
[Compatibility register]
Reg (06) h←(14) h Write [year]
Reg (05) h←(04) h Write [month]
Reg (04) h←(18) h Write [day]     *2

- Set day of week
[Compatibility register]
Reg (03) h←(20) h Write [day of week]

- Set hour/minute/second
[Compatibility register]
Reg (02) h←(15) h Write [hour]
Reg (01) h←(30) h Write [minute]
Reg (00) h←(00) h Write [second]     *3

*4
Settings check OK?     No

Yes

Reset sub-second counter
If EVIN terminal is switched from "L" to "H,"
reset occurs and clock is restarted     *5

*1) Set ERST bit to "1" to put sub-second counter in reset standby mode. Then put in external event input waiting mode.
*2), *3) Data is BCD (binary coded decimal) code.
*4) Read written data to see if desired data is written. (Can be omitted)
*5) If the desired external event occurs at the EVIN terminal, the sub-second clock counter is reset.
The clock counter is instantly reset, regardless of the chatter removal setting for EVIN terminal input as specified in the ET0 and ET1 bits.
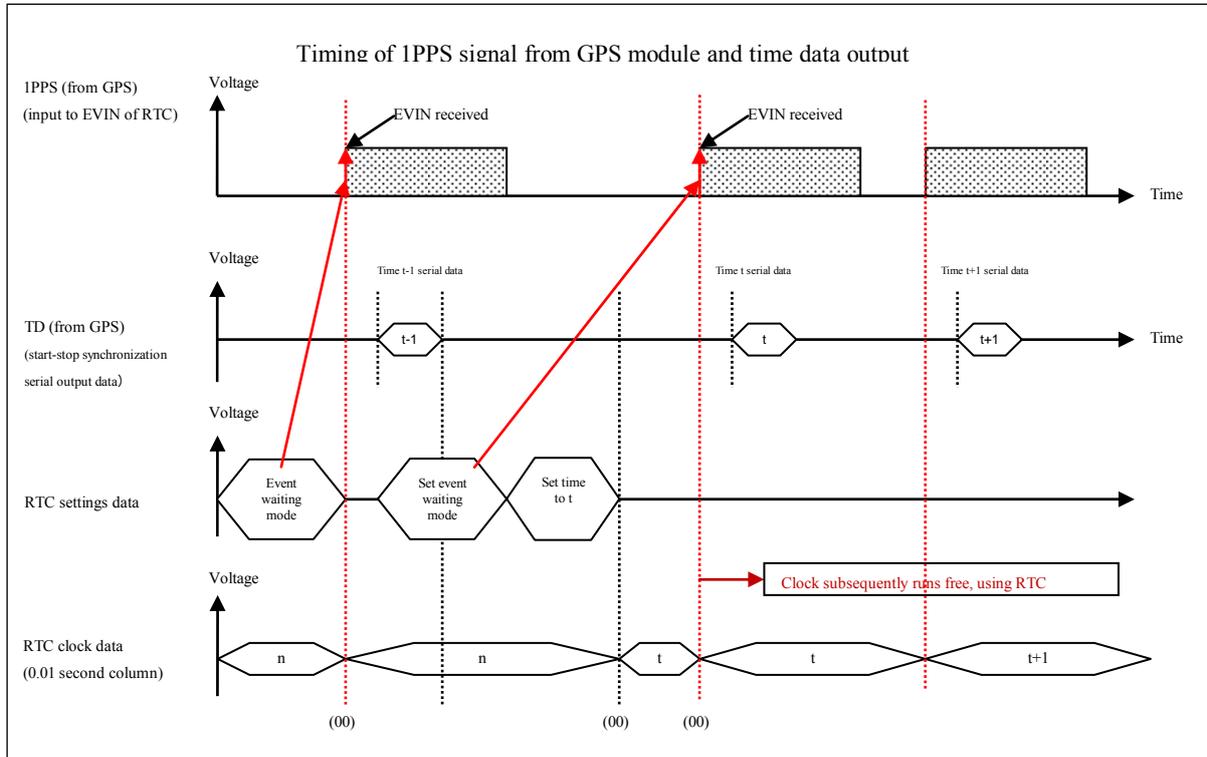(However, there will be a delay of tens of ns because of internal element delay.)

• High-accuracy time adjustment setting synchronized with 1PPS signal

Hardware-based time adjustment with the ERST bit inputs the 1PPS signal (Pulse per second_1Hz output signal) that comes with the GPS module, etc., as the external event. This makes it possible to receive an accurate GPS time signal to make high-accuracy time adjustment.

Below is an example of a timing chart of a 1PPS signal from a GPS module and time data output.

Timing of 1PPS signal from GPS module and time data output

**1PPS (from GPS)** (input to EVIN of RTC) — Voltage — EVIN received / EVIN received

**TD (from GPS)** (start-stop synchronization serial output data) — Voltage — Time t-1 serial data: t-1 / Time t serial data: t / Time t+1 serial data: t+1

**RTC settings data** — Voltage — Event waiting mode / Set event waiting mode / Set time to t

**RTC clock data** (0.01 second column) — Voltage — n / n / t / t / t+1 — Clock subsequently runs free, using RTC — (00) (00) (00)

Users of this function should be aware that it may not be possible to adjust the time correctly in environments where the GPS module cannot correctly receive information from a satellite.

Epson provides products that, in addition to the above-discussed high accuracy (clock accuracy) of the real-time clock modules themselves, have other functions to meet customer needs to support the building of high-accuracy time synchronization systems. Additionally, the frequency stability of all Epson real-time clock module products is adjusted and ensured upon shipping from the factory. This eliminates the need to tune the frequency during module use and helps enhance the efficiency and quality of customers' design processes.