



Real Time Clock Module

RX4111CE

Linux driver overview.

Ver-1.0

Category	General
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Document information and revision resume

■ Resume for Revision

Version	Date	Revised Contents	Page	
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1. Introduction

This document was developed by Raspberry PI3 for the EPSON RX4111CE RTC Driver.
The kernel version was developed in the environment of 4.14.76 and was written to load drivers, connect to hardware.

2. Raspberry PI 3

This is related to the setup of the Raspberry PI3 board before testing the driver.
Use raspi-config for Raspberry PI SPI settings.

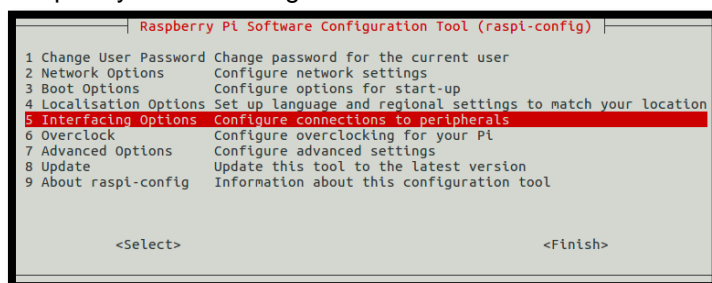


Figure 1

Select SPI.

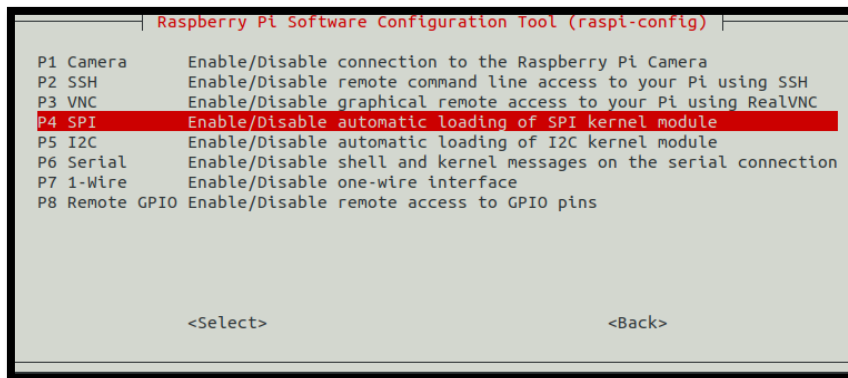


Figure 2

Select SPI to activate it.

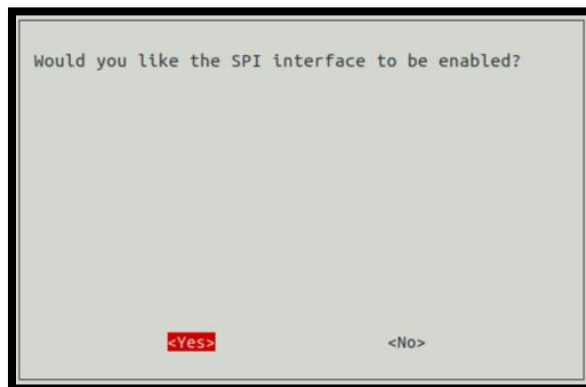


Figure 3

SPI has been activated.

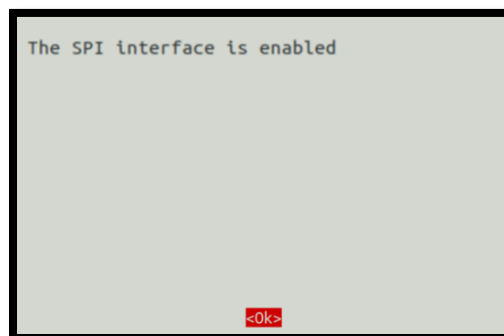


Figure 4

To use the device tree, add a dtoverlay entry to /boot/config.txt as shown below.

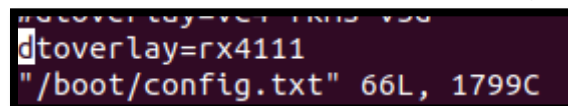


Figure 5

3. Hardware

The hardware is configured according to the table below in the RX4111CE Data Sheet.

3.2. Pin Functions

Table 1 Pin Description

Signal name	I/O	Function
CE	Input	Chip enables input pin (SS) Should be held high to allow access to the CPU. Incorporates a pull-down resistor
CLK	Input	Serial clock input pin (SCLK)
DI	Input	Data input pin (MOSI)
DO	Output	Data output pin (MISO)
FOUT	Output	Frequency output pin (CMOS) (frequency selection: 32.768 kHz, 1024 Hz, 1 Hz) When output is stopped, the FOUT pin is High impedance.
/INT	Open-Drain Output	This pin is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an N-ch open drain
V _{DD}	–	Power-supply pin Possible to supply different voltage from V _{IO}
V _{IO}	–	Interface power supply pin Input to supply the voltage same as a host
V _{BAT}	–	This is a power supply pin for backup battery Connect an EDLC, a secondary battery, a primary battery In the backup voltage range, supplied to IC, from this pin
GND	–	Ground pin

Note:

Be sure to connect a bypass capacitor rated at least 0.1 μ F between V_{DD} and GND.

For the input terminals, it is permitted for the input to be 5.5 V regardless of the V_{IO} voltage.

For the Open-Drain pin, it is permitted for the pull-up to be 5.5 V regardless of the V_{IO} voltage.

When FOUT or INT is not used, be left open in these pins. It doesn't need pull-Up/Down resistor.

Table 1 RX4111CE Pin Function

Since we tested using the Raspberry PI 3 board, the pin connection standards are explained in the Raspberry PI 3 standard.



Figure 6 Raspberry PI 3 Model B V1.2

3.1 Pin Connection

This is the connection between the RX4111CE chip and the raspberry Pi 3 board.








RX4111CE	Raspberry PI3	
VDD	PIN 01, 3.3v	
GND	PIN 09, Ground	
/INT	PIN 13, GPIO27	
SPI_MOSI	PIN 19, GPIO10	
SPI_MISO	PIN 21, GPIO09	
SPI_CLK	PIN 23, GPIO11	
SPI_CE0_N	PIN 24, GPIO08	

Table 2





















Raspberry Pi 3 GPIO Header					
Pin#	NAME		NAME	Pin#	
01	 3.3v DC Power		DC Power 5v	02	
03	GPIO02 (SDA1 , I ² C)		DC Power 5v	04	
05	GPIO03 (SCL1 , I ² C)		Ground	06	
07	GPIO04 (GPIO_GCLK)		(TXD0) GPIO14	08	
09	 Ground		(RXD0) GPIO15	10	
11	GPIO17 (GPIO_GEN0)		(GPIO_GEN1) GPIO18	12	
13	 GPIO27 (GPIO_GEN2)		Ground	14	
15	GPIO22 (GPIO_GEN3)		(GPIO_GEN4) GPIO23	16	
17	3.3v DC Power		(GPIO_GEN5) GPIO24	18	
19	 GPIO10 (SPI_MOSI)		Ground	20	
21	 GPIO09 (SPI_MISO)		(GPIO_GEN6) GPIO25	22	
23	 GPIO11 (SPI_CLK)		(SPI_CE0_N) GPIO08	24	
25	Ground		(SPI_CE1_N) GPIO07	26	

Figure 7

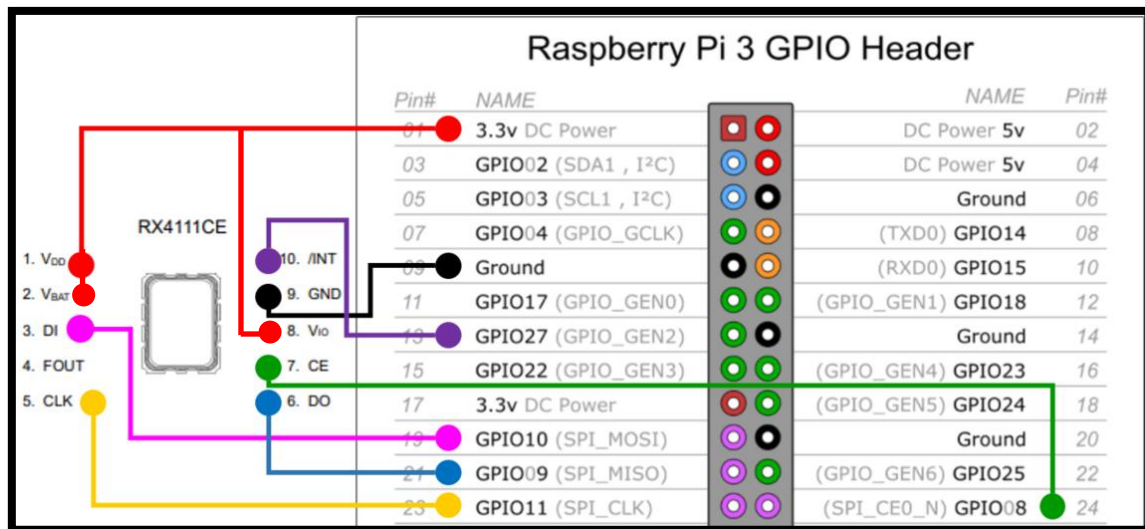


Figure 8

4. Software

Requires driver compilation, device tree modification, and compilation.

Driver is set to be compiled in the form of modules,

The device tree is include in the kernel for compile and use.

4.1 Device Tree

The device tree used an overlay of raspberry pi.

Add the rx4111.dtbo entry to the arch/arm/boot/dts/overlays/Makefile file.

rx4111.dtbo

Copy the compiled rx4111.dtbo file to the /boot/overlay directory.

And reboot to apply the device tree.

```
// Device tree overlay for SPI RTC connected RX4111CE
/dts-v1/;
/plugin/;

/ {
    compatible = "brcm,bcm2835", "brcm,bcm2708", "brcm,bcm2709";

    fragment@0 {
        target = <&spidev0>;
        __overlay__ {
            status = "disabled";
        };
    };

    fragment@1 {
        target = <&gpio>;
        __overlay__ {
            rx4111_pins: rx4111_pins {
                brcm,pins = <27>; // interrupt pin
            };
        };
    };
};
```



```

        brcm,function = <0>; //input
        brcm,pull = <2>; // pull-up

    };
};

};

fragment@2 {
    target = <&spi0>;
    __overlay__ {
        #address-cells = <1>;
        #size-cells = <0>;
        status = "okay";

        rx4111: rx4111@0 {
            compatible = "epson,rtc-rx4111";
            reg = <0>; /* CE0 */
            spi-max-frequency = <4000000>;
            pinctrl-names = "default";
            pinctrl-0 = <&rx4111_pins>;
            interrupt-parent = <&gpio>;
            interrupts = <27 2>; /* high-to-low edge triggered */
            irq-gpios = <&gpio 27 0>;
            spi-cpol;
            spi-cpha;
            spi-cs-high;
            status = "okay";
        };
    };
};

__overrides__ {
    interrupt = <&rx4111_pins>,"brcm,pins:0",
               <&rx4111>,"interrupts:0",
               <&rx4111>,"irq-gpios:27";
};
};

```

4.2 Device Driver

If the driver has been built statically in the kernel, nothing has to be done. If it is built as a module, then load it with

```
$ insmod rtc-rx4111.ko
```

On initialization, the driver will log the following message

```
$ dmesg | grep rtc-rx4111
```

```

[286380.182492] rtc-rx4111 spi0.0: SPI settings: bits_per_word: 8, max_speed_hz: 4000000, mode: 7h
[286380.182899] rtc-rx4111 spi0.0: rtc core: registered rtc-rx4111 as rtc0
[286380.182910] rtc-rx4111 spi0.0: IRQ 169 supplied

```

Figure 9

This means that rtc0 is the RX4111 rtc.