3 Axis Accelerometer: M-A370AD1

Features

- Ultra-low noise, surpassing USGS New High Noise Model [1] 0.02 µG/√Hz typ. (1 Hz ~ 10 Hz)
- High bias stability for highly accurate tilt measurement
  ± 0.5 mG max. (Temperature Error - 30 °C ~ + 85 °C)
  ± 0.1 mG typ. (Bias Repeatability for 1 year, 25 °C)
- High-precision sensitivity that do not require calibration
  Flat frequency response : ± 0.4 dB
  Flat phase : ± 0.1 °
  Low sensitivity error : ± 500 × 10^{-6}
- High dynamic range without measurement range switching : ± 10 G (170 dB)
- 3-axis digital output SPI / UART that is not easily affected by noise
- Sensitivity self-diagnosis test function
- GNSS synchronization by 1 PPS (Pulse Per Second)
- Sampling synchronization with low jitter external trigger

Application

- Seismic measurement, Resource exploration,
  Tilt measurement, Structural Health Monitoring (SHM),
  Vibration analysis / control / stabilization

Typical Performance Characteristic

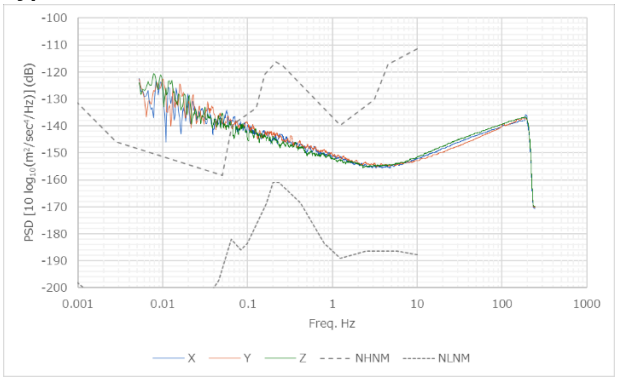


Figure Noise Density

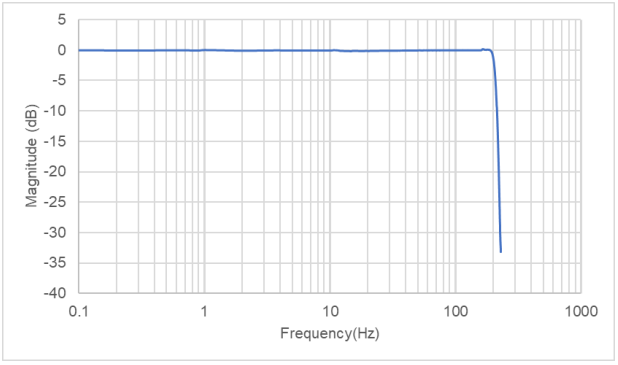


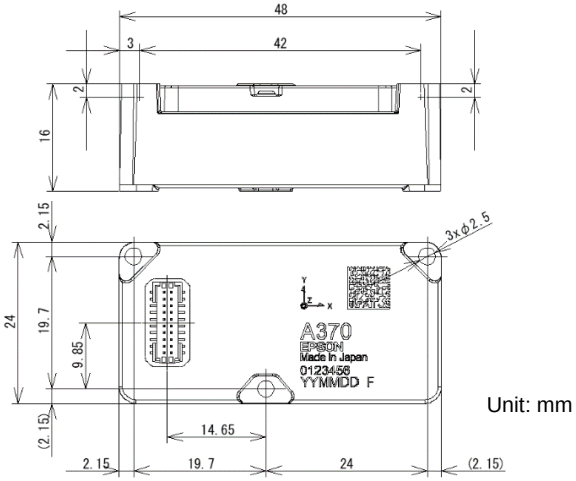
Figure Frequency Response

Description

The M-A370 is a three axis digital output accelerometer featuring ultra-low noise, high stability, and low power consumption using fine processing technology of Quartz.

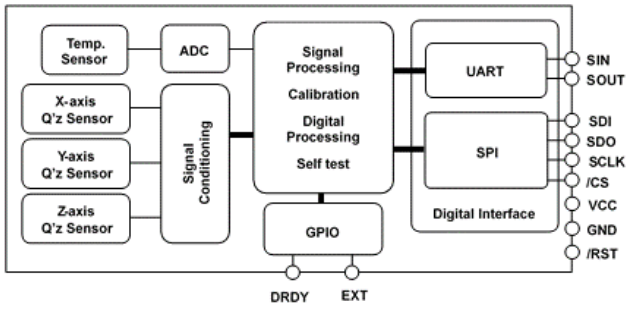
Incorporating high accuracy, wide bandwidth, and durability, the versatile M-A370 is well suited to a wide-range of challenging applications such as Seismic measurement, Resource exploration, Tilt measurement, and Structural Health Monitoring (SHM).

Outline Dimentions



Unit: mm

Block Diagram



[1] Peterson, J., "Observations and Modeling of Seismic Background Noise", USGS Open-File Report 93-322, 1993

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Revision History

Rev. No.	Date	Page	Description
20250520	2025/5/20	ALL	New release.
20250903	2025/9/3	8	Correction of product model number

Ordering Information

The product can be ordered with the following numbers. Please inquire separately about details.

Product Model Number	Product Name	Comments
X2F000091000100	M-A370AD1	This product.

Evaluation tools

Evaluation tools can be provided for this product. Please inquire separately about details.

Product Model Number	Product Name	Comments
X2H000021000200	M-G32EV041	USB Evaluation Board for Accelerometer/IMU. Option to connect M-A370 to the USB port of a PC.
X2H000021000300	M-G32EV051	Relay Board for Accelerometer/IMU. Option to reduce the vibration effect of the USB cable.
-	Vibration Data Logger	Accelerometer/Vibration sensor Logger Software. For more information, please contact us.
-	Vibration Data Viewer	This software is designed to graphically display and analyze waveform data output from the Vibration Data Logger. For more details, please contact us.

Design Support Information

https://www.epson.jp/prod/sensing_system/support/

Symbols

RoHS Compliant	**● Compliant with the EU RoHS directive.** * About products without the Pb-Free label Product terminals are lead-free but the internal components of the product contain lead (high melting point solder lead as well as the lead contained in the glass of an electronic component are both not applicable under the EU RoHS directive).

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2025.5

Prohibited Items

This product is a precision instrument. Improper handling may cause damage.
Before use, please ensure to review the Prohibited Items and Chapter 8 Handling Notes of this datasheet.

Do not drop the sensor.
Even a fall from a height of 50 mm may cause damage.

Do not strike the sensor or its surroundings with a hammer.
Strong vibrations may cause damage.

Do not install the sensor using an electric screwdriver.
Strong vibrations may cause damage.

Do not connect or disconnect connectors while the sensor is powered.
Unexpected potential differences may damage the IC.

When handling the sensor, take anti-static measures.
Static electricity may damage the IC.

Precautions

Depending on the application, attention must be paid to the installation method of the product. Before use, please ensure to review the Precautions and Chapter 8 Handling Notes of this datasheet.

Beware of structural resonance excitation.
This product has structural resonance around 450 Hz. If structural resonance is excited, the input signal may be excessively amplified, making accurate measurement impossible.

Beware of power noise and GND noise contamination.
Noise may be superimposed on the measurement data. To suppress power noise contamination, it is recommended to use a linear power supply. Also, connect the case's Frame Ground to the sensor's GND pins (3, 4, 8, 15).

Beware of contact between the product case and electronic components.
The product case is conductive. If the case contacts electronic components, it may cause a short circuit. Do not mount electronic components on the case side of the connection board. If contact between the board and the case is expected, take measures such as inserting an insulating sheet.

Beware of the installation posture of this product.
To achieve the best performance, the XY axes must be installed within ± 0.035 rad (± 2 °). Install within the recommended angle range for the following applications:
・When measuring environmental vibrations below 1 µG/√Hz
・When XYZ axes synchronization within 5 µs is required
For applications other than those listed above, there are no restrictions on the installation posture.

Export Information

This product is subject to export regulations as defined by the "Foreign Exchange and Foreign Trade Act." When exporting, please follow the relevant laws and regulations of the region and complete the necessary procedures.

1. Specifications

1.1. Absolute Maximum Ratings

Table 1.1 Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
V_{CC} to GND	- 0.3		3.6	V
Digital Input Voltage to GND	- 0.3		V_{CC} + 0.3	V
Digital Output Voltage to GND	- 0.3		V_{CC} + 0.3	V
Storage Temperature Range	- 40		85	°C
Acceleration (Half-sine 0.2 ms) *1			500	G
Sensor installation orientation	No restrictions			-

*1) Shock resistance is based on test results under specific conditions and does not guarantee resistance to all shocks. When handling the sensor, avoid subjecting it to shocks as much as possible.

1.2. Recommended Operating Condition

Table 1.2 Recommended Operating Condition

Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC} to GND		3.15	3.3	3.45	V
Digital Input Voltage to GND		GND		V_{CC}	V
Digital Output Voltage to GND		- 0.3		V_{CC} + 0.3	V
Operating Temperature Range		- 30		85	°C
Start up Time	Power-on to start output.			900	ms
	Warm-up period for best performance.		300		s
Sensor installation orientation *1	Angle of XY axis	- 0.035 (- 2)		+ 0.035 (+ 2)	rad °

*1) There are no restrictions on the installation posture of this product, but it achieves optimal performance when the XY axes is within ± 0.035 rad (± 2 °). For the following applications, install within the recommended angle range:
- High-precision vibration measurement with environmental vibrations below 1 µG/√Hz
- XYZ axes synchronization within 5 µs

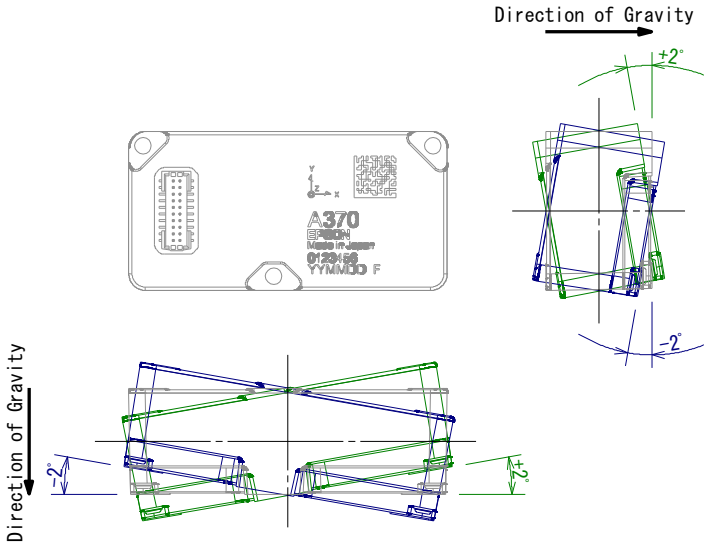


Figure 1.1 Recommended installation orientation (Angles are exaggerated in this figure, Third-angle projection)

1.3. Performance and Electrical Specifications

Table 1.3 Sensor Specifications

Conditions: T_a = - 30 °C ~ +85 °C, Vcc = 3.15 V ~ 3.45 V, ≤ ± 1 G, unless otherwise noted.

Parameter	Test Conditions / Comments	Min.	Typ.	Max.	Unit
ACCELERATION					
Sensitivity					
Output Range	f = DC ~ 210 Hz	- 10		+ 10	G
Scale Factor	2^{-24} G/LSB		0.06		µG/LSB
Sensitivity Error	25 °C, -1 G ~ 1 G		± 500		x 10^{-6}
Nonlinearity	25 °C, -1 G ~ 1 G, Best fit straight line			± 0.03	%
Cross Axis Sensitivity	No alignment correction		± 0.2		%
Misalignment	25 °C			± 0.1	°
Bias					
Initial Error	25 °C			± 2.0	mG
Bias Repeatability *4	One year after shipment, 25 °C, V_{CC} = 3.3 V, Average		± 0.1		mG
	One year after shipment, 25 °C, V_{CC} = 3.3V, Sigma		0.15		mG
Bias Temperature Error	Bias offset change from 25°C reference			± 0.5	mG
Temperature sensitivity			± 0.1		mG/°C
Noise					
Noise Density	25 °C, Average, f = 1 Hz ~ 10 Hz		0.02	0.04	µG/√Hz, rms
Cantilever Resonance Frequency *1	25 °C, V_{CC} = 3.3 V		450 Hz		Hz
VRC	at 50 Hz, 25 °C, V_{CC} = 3.3 V			± 50	µG/G^2
Frequency Property					
Frequency Range	User selectable	9		210	Hz
TILT ANGLE					
Sensitivity					
Output Range	f = DC ~ 210 Hz			± 1.047 (± 60)	rad (°)
Scale Factor	2^{-29} rad/LSB		0.002		µrad/LSB
Nonlinearity	+25 °C, ± 45 °	- 0.03		+ 0.03	%
Misalignment	25°C			± 1.745 (± 0.1)	mrad (°)
Bias					
Bias Repeatability	One year afer shipment, 25 °C, V_{CC} = 3.3 V		± 0.1 (± 0.006)		mrad (°)
Bias Temperature Error	25 °C			± 0.5 (± 0.029)	mrad (°)
Noise					
Noise Density	25 °C, Average, f = 1 Hz ~ 10 Hz		0.02	0.04	µrad/√Hz, rms
TEMPERATURE SENSOR					
Output Range		- 30		+ 85	°C
16-bit Scale Factor *2	Output = 2634 (0x0A4A) at 25 °C		- 0.0037918		°C/LSB
RELIABILITY					
MTTF*3	25 °C	87,600			h

*1) Please make sure that a vibration on this product around the resonance frequency does not exceed 5 mG. Please take an appropriate action (e.g. installing a damper mechanism) if it exceeds 5 mG.

*2) This is a reference value used for the internal temperature correction, and is not guaranteed to accurately output the interior temperature.

*3) Based on the test results, the estimated value is determined under the condition of an 80 % reliability level.

*4) Estimated value from accelerated testing results.

Note) The values in the specifications are based on the data calibrated at the factory. The values may change according to the way the product is used.

Note) The Max/Min value is the maximum/minimum value of the design or factory shipment examination, unless otherwise specified.

Note) The calibrated standard 1 G gravitational acceleration value is 9.80665 m/s^2.

Table 1.4 Interface Specifications

T_a = 25 °C, V_{CC} = 3.3 V, unless otherwise noted.

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS[*1]					
Positive Trigger Voltage	Schmitt	1.37		2.29	V
Negative Trigger Voltage	Schmitt	0.69		1.24	V
Hysteresis Voltage	Schmitt	0.53			V
Input Current	VI = V_{CC} or GND		0.5		µA
Input Capacitance			2.5		pF
RST Low Pulse Width		100			ms
Pull-up resistor			220		kΩ
Ext.Trigger Input Width, t_{ETW}		1			µs
Ext.Trigger Input Cycle, t_{ETC}		1		20	ms
Ext.Trigger Jitter, t_{ETJ}	ADC's completion to Ext.Trigger input	0		5	µs
1 PPS Input Cycle, t_{PPS}		1 - 10^{-5}	1	1 + 10^{-5}	s
Ext.Trigger Delay time[*3], t_{ETD}	Ext.Trigger input to DRDY asserted Long-period filter = disable			740	µs
Internal Timer Delay Time[*3], t_{ITD}	Internal Timer input to DRDY asserted Long Period Filter = disable			430	µs
DIGITAL OUTPUTS[*1]					
Output High Voltage	ISOURCE = 20 µA	V_{CC} - 0.1			V
Output Low Voltage	ISINK = 20 µA			0.1	V
FUNCTIONAL TIMES[*2]	Time until data is available				
Power-On Start-Up Time[*4]				900	ms
Reset Recovery Time[*4]				970	ms
Flash Backup Time				310	ms
Flash Reset Time				2300	ms
Self Test Time	ACC Test , TEMP Test , VDD Test			200	ms
	Sensitivity Test			13	s
	Flash Test			5	ms
Filter Setting Time	Built-In FIR Filter			4	ms
	User FIR Filter			100	ms
User Filter Write Cycle, t_{UWC}				7	ms
User Filter Read Cycle, t_{URC}				500	us
Sampling Start Time	Configuration mode to Sampling mode			3	ms
Sampling Stop Time	Sampling mode to Configuration mode			1	ms
Sleep Wake-up Time				16	ms
Output Data Rate		50		1000	Hz
Clock Accuracy				± 0.001	%
Power Supply Current	Acceleration output, Average		36.3	43.0	mA
	Tilt angle output, Average		36.3	43.0	mA
	Sleep mode		2.2	3.0	mA

*1) Digital I/O signal pins operate at 3.3 V inside the unit.

*2) These specifications do not include the effect of temperature fluctuation and response time of the internal filter.

*3) It is not included the group delay of the built-in filter.

*4) Avoid accessing the interface during startup and reinitialization.

*5) The synchronization accuracy depends on the precision of the 1 PPS signal.

Note) These parameters are not included in the factory test items but these characteristics are confirmed.

1.4. Timing Specifications

Table 1.5 SPI Timing Specifications

T_a = 25 °C, V_{CC} = 3.3 V, unless otherwise noted.

Parameter	Description	Min.	Typ.	Max.	Unit
NORMAL MODE					
fSCLK		0.01		2.0	MHz
tSTALL	Stall period between data	20			µs
tWRITERATE	Write rate	40			µs
tREADRATE	Read rate	40			µs
BURST MODE					
fSCLK		0.01		2.0	MHz
tSTALL1	Stall period between data	45			µs
tSTALL2	Stall period between data	0			µs
tREADRATE2	Read rate	8			µs
COMMON					
tCS	Chip select to clock edge	10			ns
tDAV	SO valid after SCLK edge			80	ns
tDSU	SI setup time before SCLK rising edge	10			ns
tDHD	SI hold time after SCLK rising edge	10			ns
tSCLKR, tSCLKF	SCLK rise/fall times			20	ns
tDF, tDR	SO rise/fall times			20	ns
tSFS	high after SCLK edge CS	80			ns

Note) These parameters are not included in the factory test items but these characteristics are confirmed.

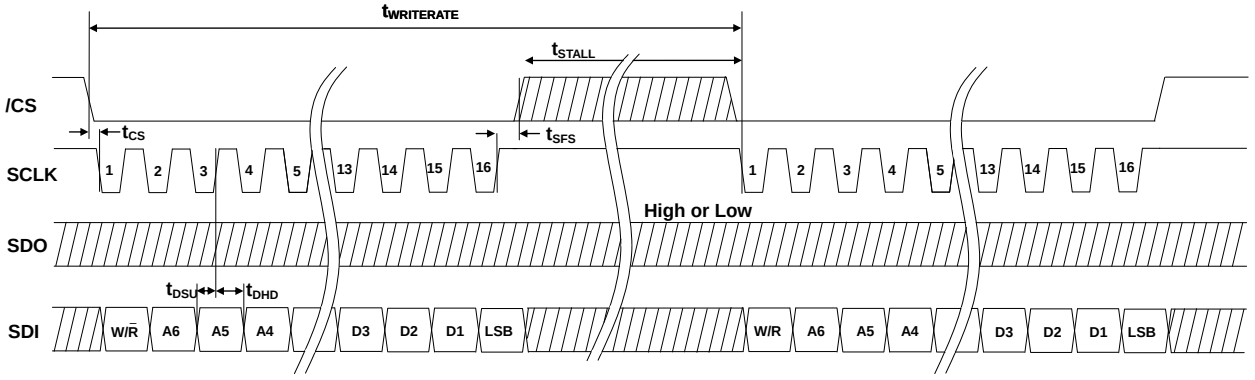


Figure 1.2 SPI Write Timing and Sequence

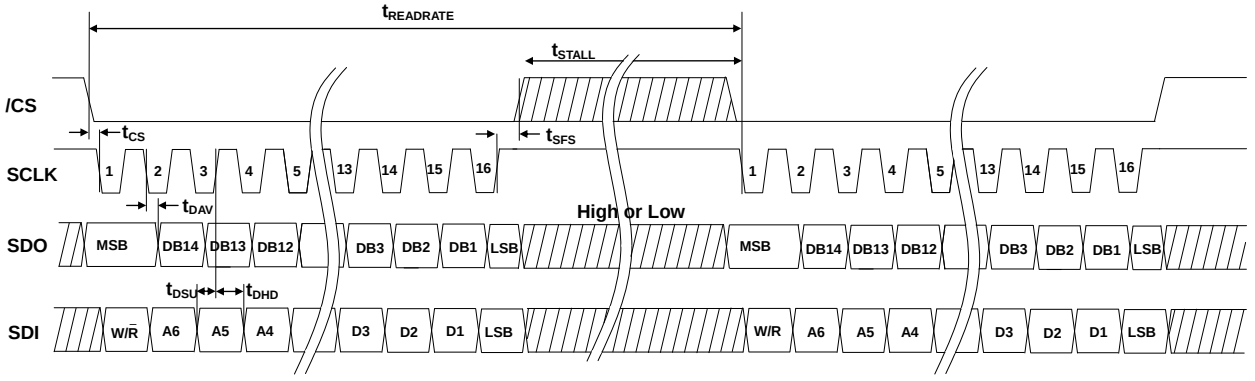


Figure 1.3 SPI Read Timing and Sequence

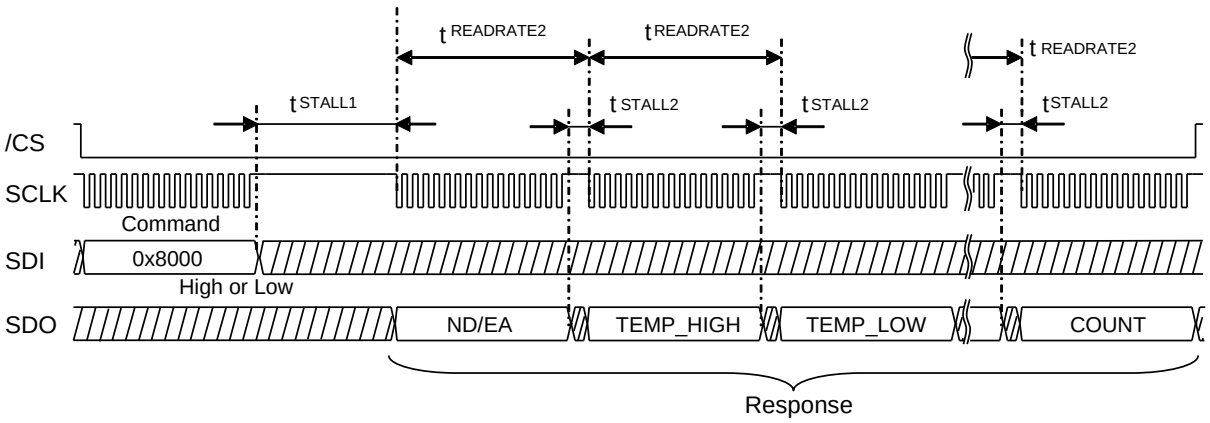


Figure 1.4 SPI Read Timing and Sequence (BURST MODE)

1.5. Socket Pin Layout and Functions

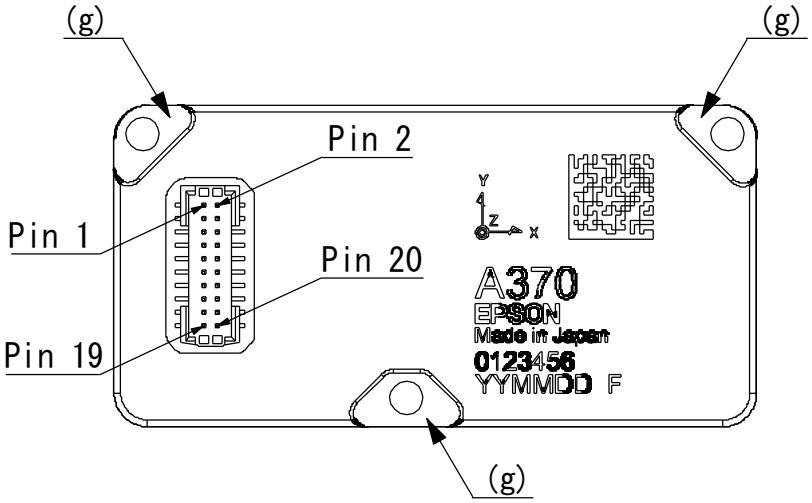


Figure 1.5 Socket Pin Assignment

Precautions (Important)

- **Frame Ground (g) must be connected to one of the GND pins (3, 4, 8, or 15).**
- **Do not insert or remove the socket while the power is on. Otherwise, overvoltage or overcurrent may be applied to the socket pins, which may damage the circuitry inside the product.**
- **Do not force the connector into the socket when the socket pins are not in the proper position. Otherwise, the socket guide may be damaged or the pins may be bent.**

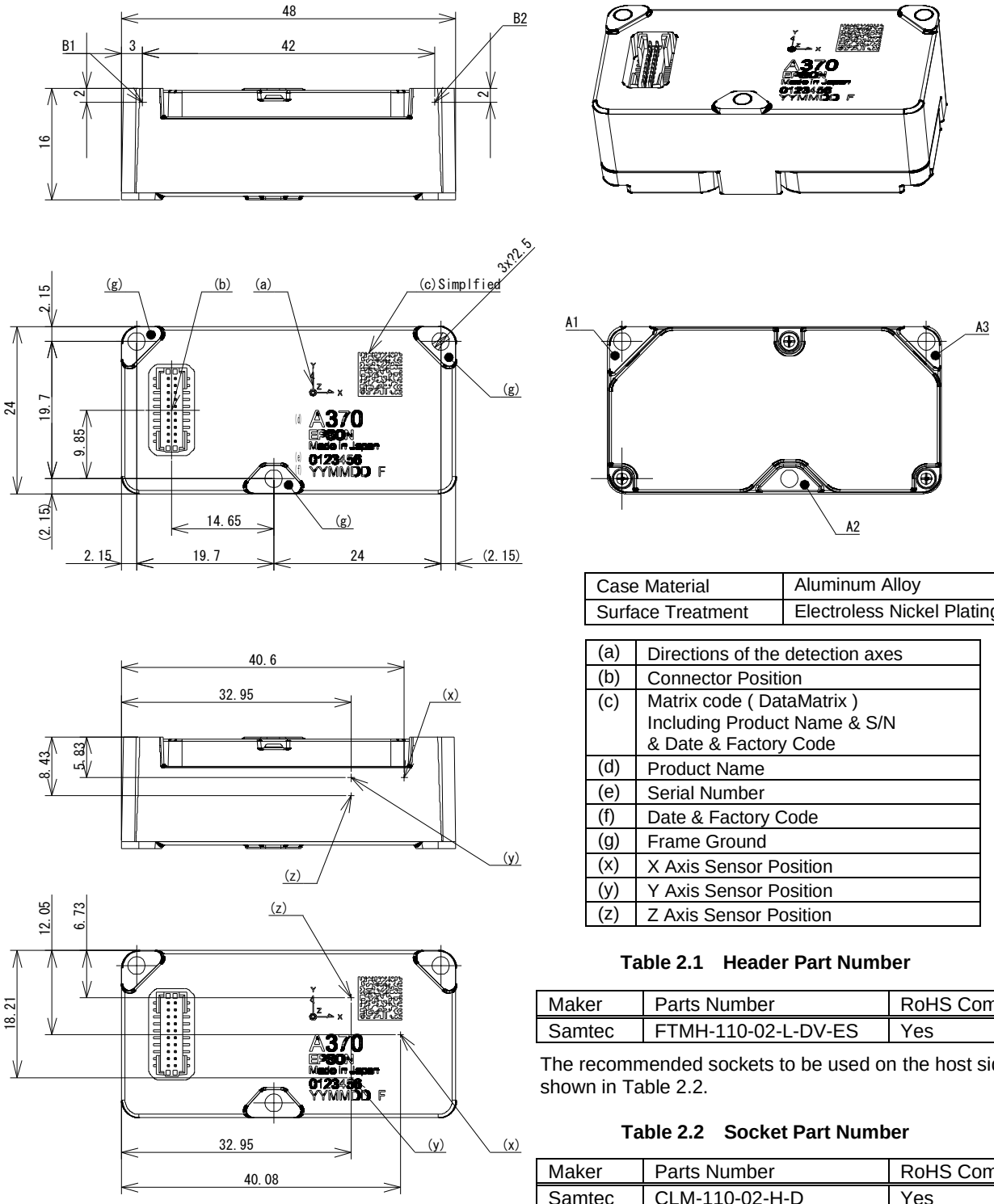
Table 1.6 Pin Function Descriptions

Pin No.	Mnemonic	Type[*1]	Description
1	SCLK	I	SPI Serial Clock [*2]
2	SDO	O	SPI Data Output [*2]
5	SDI	I	SPI Data Input [*2]
6	/CS	I	SPI Chip Select [*2]
7	SOUT	O	UART Data Output [*2]
9	SIN	I	UART Data Input [*2]
13	DRDY	O	Data Ready [*3]
14	EXT	I	External Trigger Input [*4] (Sleep Wakeup Input)
16	/RST	I	Reset [*5]
10, 11, 12	VCC	S	Power Supply 3.3 V
3, 4, 8, 15	GND	S	Ground [*6]
17, 18, 19, 20	NC	N/A	Do Not Connect

*1) Pin Type I: Input, O: Output, I/O: Input/Output, S: Supply, N/A: Not Applicable
*2) Please connect either SPI or UART. Connecting both SPI and UART at the same time may cause malfunction. Please connect unused input pins to V_{CC} via a resistor.
*3) Please refer to **DRDY_ON** of register: MSC_CTRL [0x02 (W1)], bit [2] for pin function selection.
*4) Please refer to **EXT_SEL** of register: MSC_CTRL [0x02 (W1)], bit [7:6] for pin function selection.
*5) When /RST pin is not used, fix it to High (V_{CC}) level via a resistor.
*6) Please connect Frame Ground (g) to any GND pin (No.3, 4, 8, 15).
Note) All input pins have weak pull up resistors inside this product.

2. Mechanical Dimensions

2.1. Outline Dimensions



Case Material	Aluminum Alloy
Surface Treatment	Electroless Nickel Plating

(a)	Directions of the detection axes
(b)	Connector Position
(c)	Matrix code (DataMatrix) Including Product Name & S/N & Date & Factory Code
(d)	Product Name
(e)	Serial Number
(f)	Date & Factory Code
(g)	Frame Ground
(x)	X Axis Sensor Position
(y)	Y Axis Sensor Position
(z)	Z Axis Sensor Position

Table 2.1 Header Part Number

Maker	Parts Number	RoHS Compliant
Samtec	FTMH-110-02-L-DV-ES	Yes

The recommended sockets to be used on the host side are shown in Table 2.2.

Table 2.2 Socket Part Number

Maker	Parts Number	RoHS Compliant
Samtec	CLM-110-02-H-D	Yes
Samtec	CLM-110-02-L-D	Yes

Figure 2.1 Outline Dimensions (millimeters)

*1) This product is calibrated based on the surfaces A1, A2, A3, and B1, B2.
*2) In order to demonstrate the performance of the product properly, please fix surfaces A1, A2, A3 to rugged parts with M2 screw.
*3) When high connection reliability is required, please tighten this product together with the board on which the connector is mounted.

3. Typical Performance Characteristics

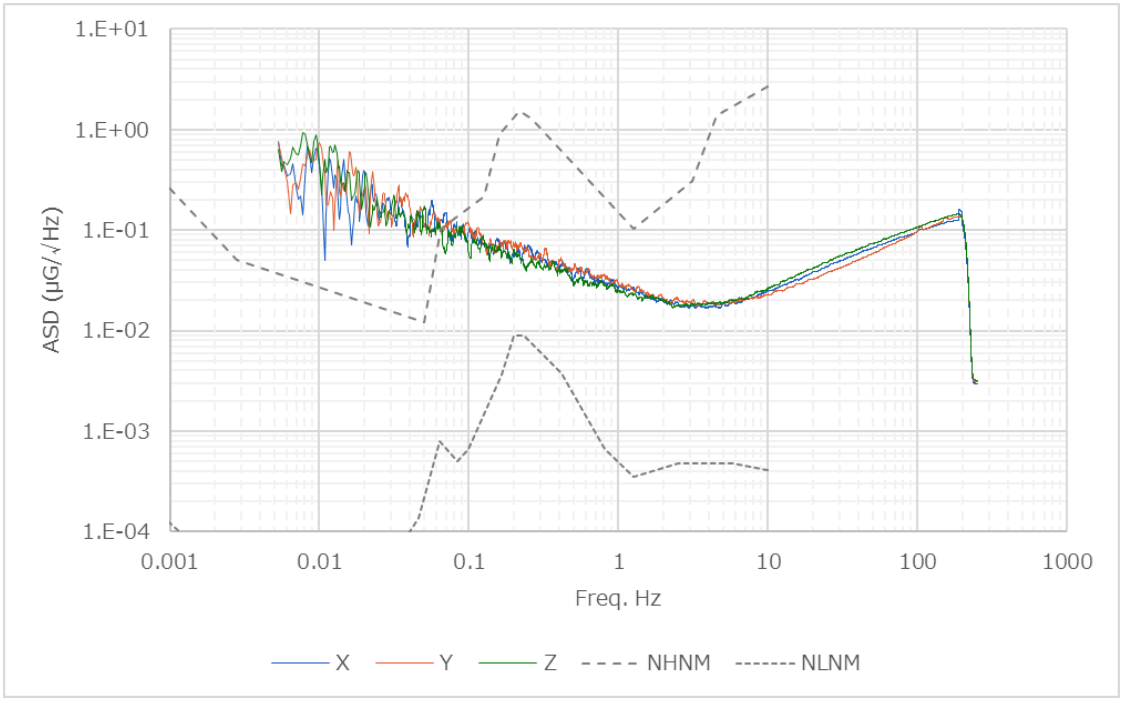


Figure 3.1 Noise Density Characteristic (μG/√Hz)

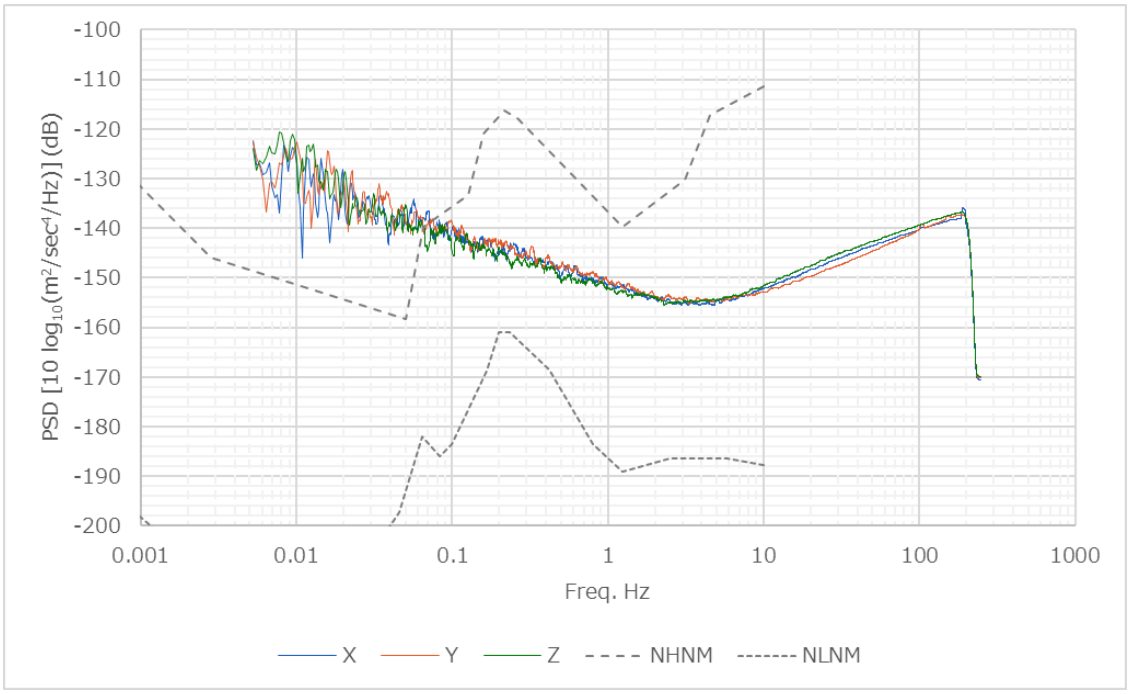


Figure 3.2 Noise Frequency Characteristic (dB)

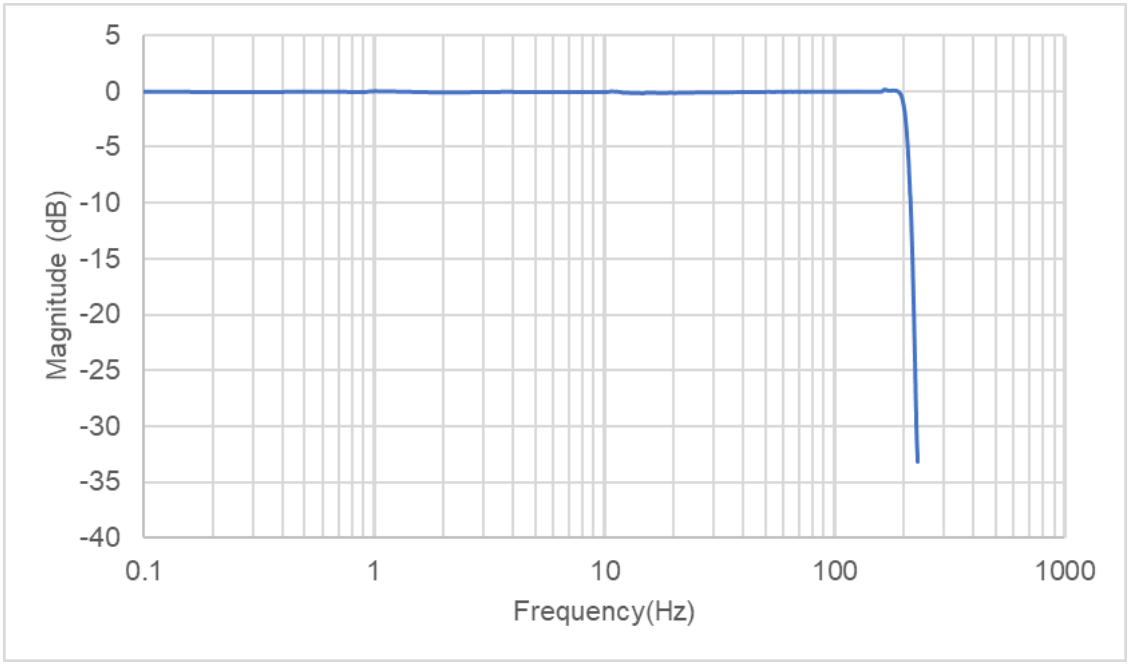


Figure 3.3 Frequency Response

Note) The above graph is a typical example of the product characteristics, and is not guaranteed by the specification.

ASD (Amplitude Spectrum Density)
PSD (Power Spectrum Density)

4. Basic Operation

4.1. Connection To Host

The device supports two types of serial interface: UART and SPI. Only one interface type should be selected and used at any given time (not both). Connecting both SPI and UART at the same time may result in malfunction of the device. The example wiring connection is provided below as a reference.

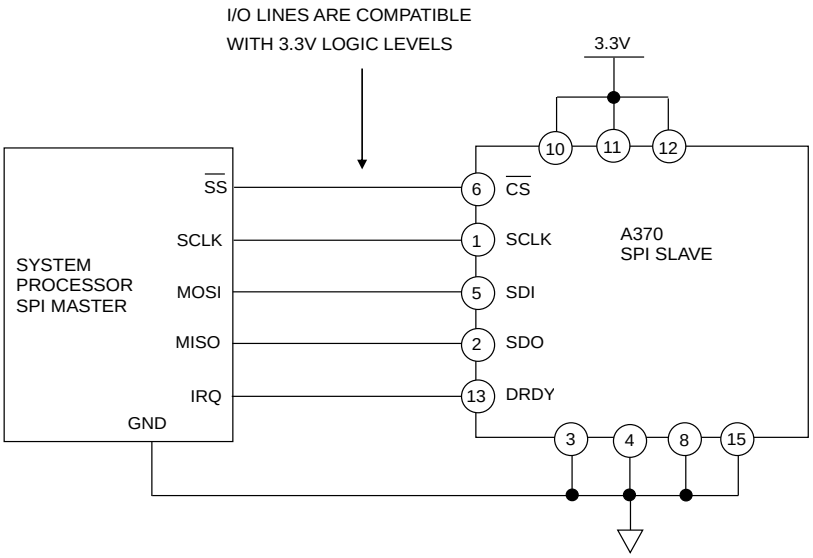


Figure 4.1 SPI Connection

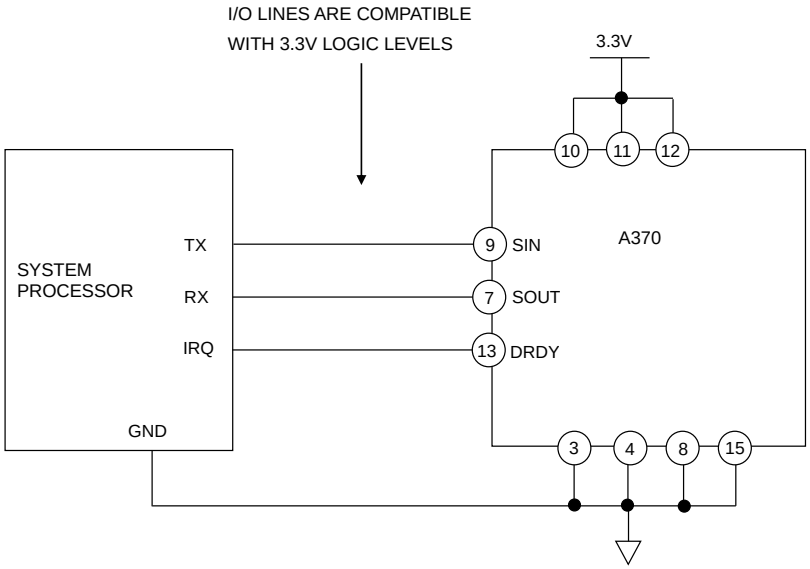


Figure 4.2 UART Connection

4.2. Operation Mode

The following three operational modes are available in the device. Only when UART is used, Sampling mode has two submodes: Manual mode and Auto mode.

(1) Configuration mode

(2) Sampling mode

- Manual mode
- Auto mode (for UART only)

(3) Sleep mode

Immediately after a hardware reset or power-on, internal initialization starts. During the internal initialization, all the register values and states of external pins are undefined. After the internal initialization is completed, the device goes into Configuration mode automatically, except when using the UART interface when **AUTO_START** and **UART_AUTO** sampling are both enabled (the device then goes into Sampling mode automatically). To change the operation mode, write to **MODE_CMD** (MODE_CTRL [0x02(W0)], bit [9:8]) (*1) and make various changes to the sensor setting in Configuration mode (*2). After configuration is completed, go to Sampling mode to read out the temperature and acceleration data. When shifting to the sleep mode, the internal circuit operation stops and the current consumption during standby can be reduced. The return time from sleep mode can be shorter than the initialization time from startup. The device can wake up from sleep mode by detecting an edge trigger on the EXT pin.

By executing software reset (Register: GLOB_CMD [0x0A (W1)], write 1 to **SOFT_RST** in bit [7]), internal initialization operation is executed regardless of the current operation mode.

When the UART interface is used, writing to **UART_AUTO** (UART_CTRL [0x08(W1)], bit [0]) can switch between Manual sampling and Auto sampling (*3). When SPI interface is used, Manual sampling must be selected. Otherwise, the device does not work properly.

*1) The following explains register notation used in this document.

For example, MODE_CTRL [0x02(W0)], bit [9:8] refers to:

- MODE_CTRL: Register Name
- [0x02(W0)]: First number is the Register Address, (W0) refers to Window Number “0”
- bit [9:8]: Bits from 9 to 8

*2) Make sure that the device is in Configuration mode when you write to the registers to configure operational settings. In Sampling mode, writing to registers is ignored except the following cases.

- Writing to **MODE_CMD** (MODE_CTRL [0x02(W0)], bit [9:8])
- Writing to **SOFT_RST** (GLOB_CMD [0x0A(W1)], bit [7])
- Writing to **WINDOW_ID** (WIN_CTRL [0x7E(W0/W1)], bit [7:0])

*3) While the device is with UART Auto sampling and sensor sampling is active, register read access is not supported. Otherwise, the sampling data transmitted with the UART Auto sampling will be corrupted by the response data from the register read.

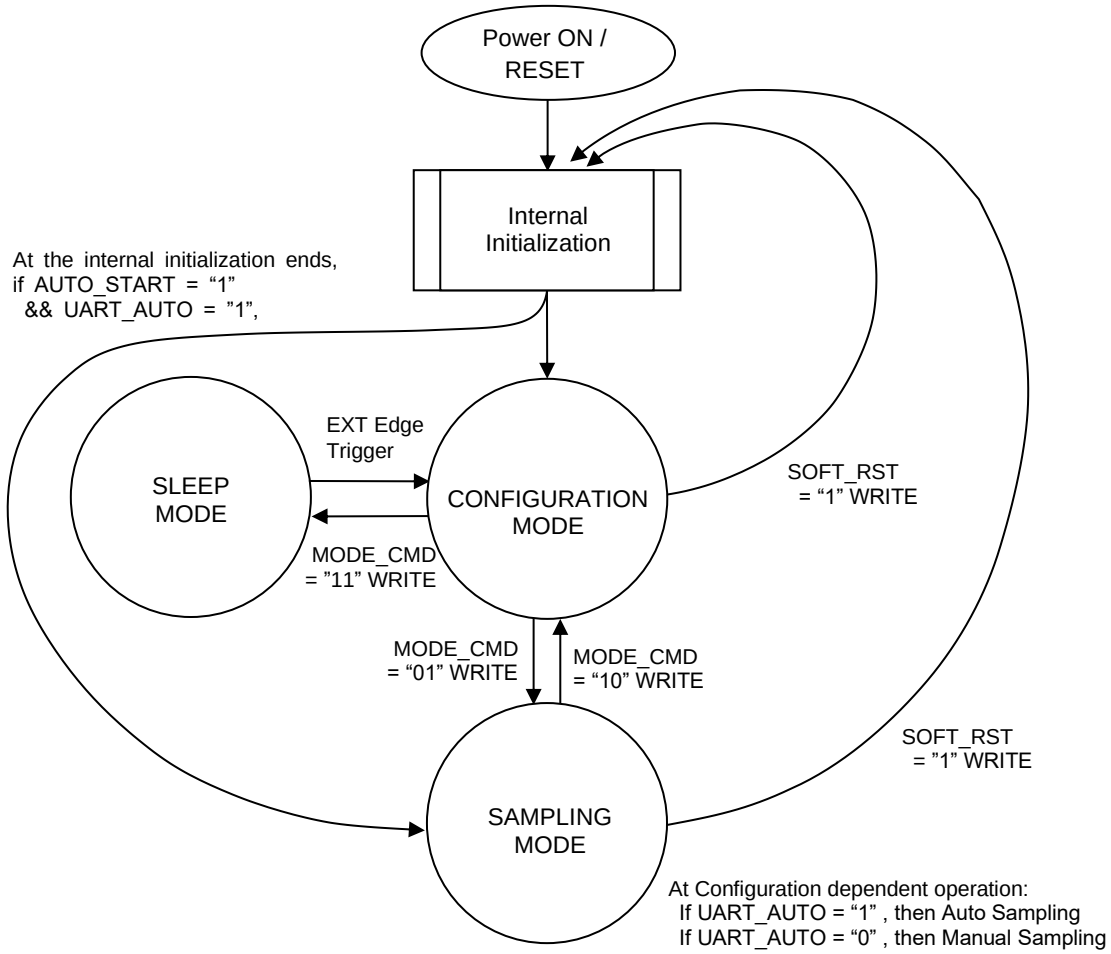


Figure 4.3 Operational State Diagram

4.3. Functional Block

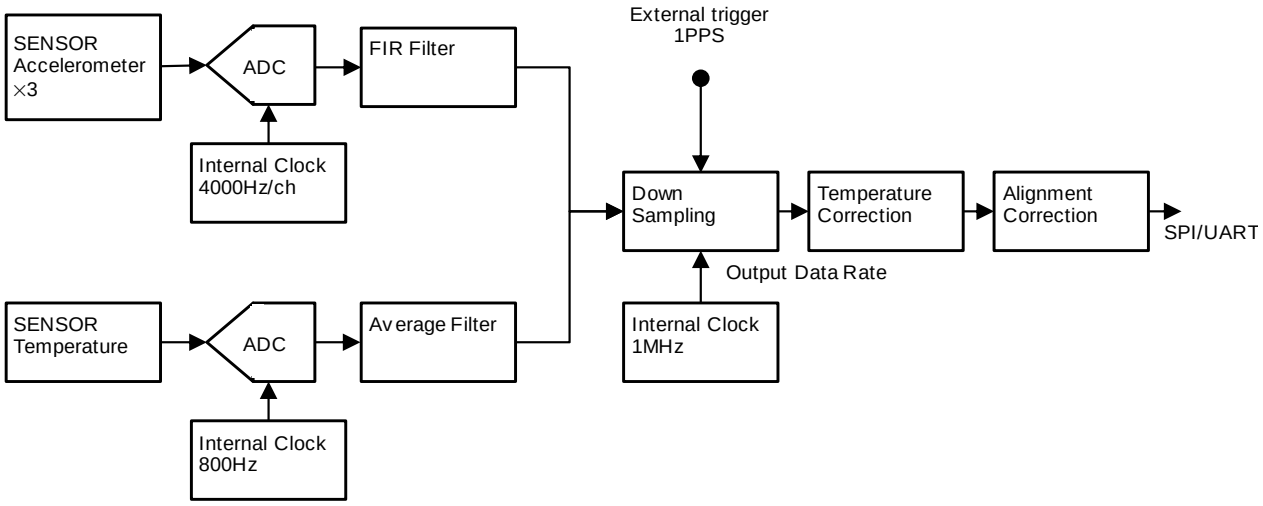


Figure 4.4 Functional Block Diagram

4.4. Data Output Timing

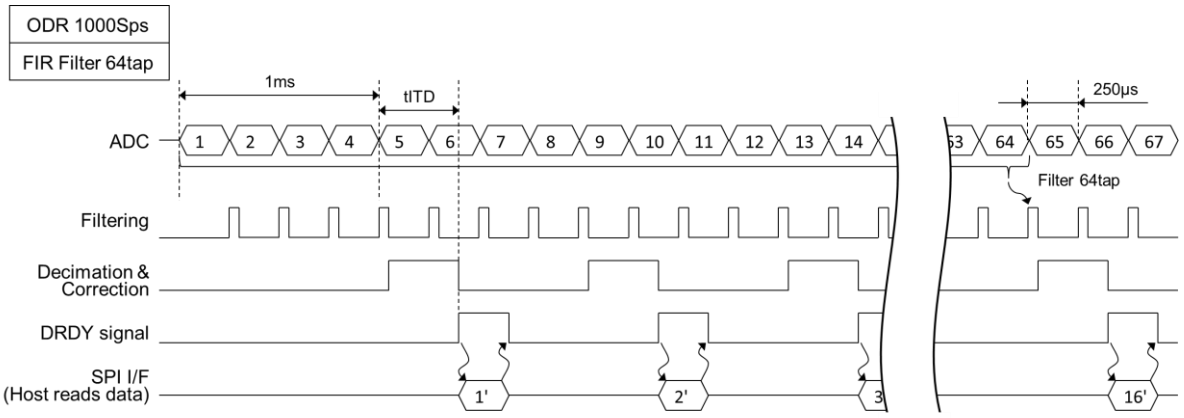


Figure 4.5 Data Output Timing

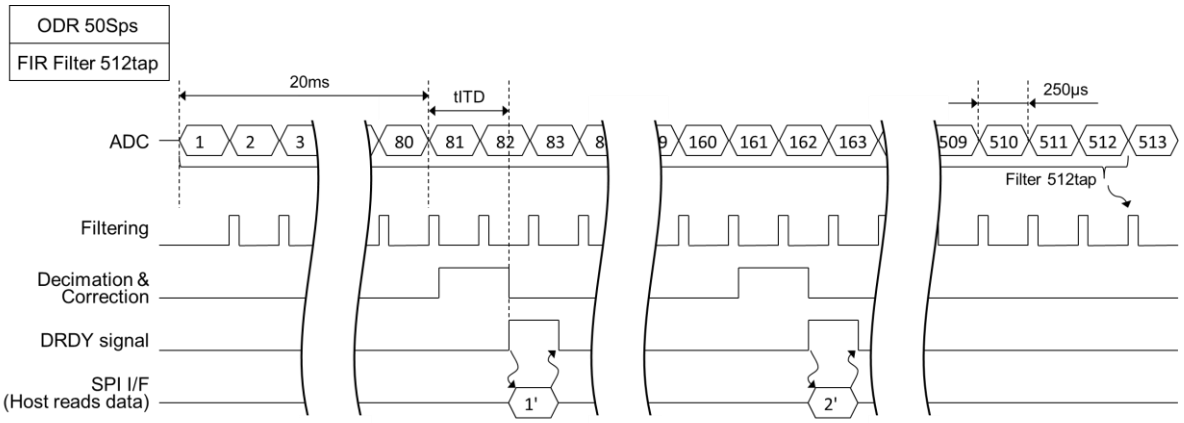


Figure 4.6 Data Output Timing

4.5. Data Ready Signal

The Data Ready Signal is asserted when one sampling cycle completes and registers are updated with new sensor values. When the sensor values are read out, the Data Ready signal becomes negated as shown in Figure 4.5 and Figure 4.6. With UART AUTO sampling enabled, the Data Ready signal becomes negated just before data is output.

The Data Ready Signal is output to the DRDY pin when the **DRDY_ON** (MSC_CTRL [0x02(W1)], bit [2]) is set to “1”. The polarity of the signal can be changed by the **DRDY_POL** of MSC_CTRL [0x02(W1)], bit [1] register.

The Data Ready Signal is the logical sum of all the ND flags corresponding to each sensor value. If all the ND flags are disabled in the **ND_EN** (SIG_CTRL [0x00(W1)], bit [15,11:9]), the Data Ready will not be asserted. On the other hand, if all the sensor values enabled in the **ND_EN** (SIG_CTRL [0x00(W1)], bit [15,11:9]) are not read out, the Data Ready signal is kept asserted and never becomes negated.

4.6. Sampling Counter

In the case of internal timer measurement, by reading COUNT [0x0A(W0)] register, the counter value, which is incremented based on the sampling completion timing of the internal Analog Front End, can be read. The count interval timing is based on the precision of the internal reference oscillator (crystal): 1/4000 Sps = 250 µs/count

For external trigger measurement and 1 PPS measurement, the counter value, which increments with each resampling timing, can be obtained by reading the register: COUNT [0x0A(W0)].

Additionally, during UART/SPI burst mode or with UART Auto sampling, the counter value can be included in the response format by setting the **COUNT_OUT** (BURST_CTRL [0x0C(W1)], bit [1]). For information about the response format, see 5.3 Data Packet Format.

4.7. Self Test

This product has the following self test functions. For information about the execution time of the self test, see “Self Test Time” in Table 1.4 Interface Specifications.

- **Acceleration Value**

  This self test function can be used to check whether the outputs of the accelerometer are within the pre-determined range and operating properly.

  The test result is OK if the absolute value of the output as a three dimensional vector is within the gravitational acceleration (0.9 G to 1.1 G).

  When performing the self test, make sure the device does not move during the test and the test is conducted in a place without vibration.

  To use this function, execute **ACC_TEST** of register: MSC_CTRL [0x02(W1)], bit [10], check the **ACC_ERR_ALL** of register DIAG_STAT1 [0x04(W0)], bit [1] for diagnostic result.

- **Sensitivity**

  To determine if there are any apparent abnormalities in the accelerometer's sensitivity, utilize environmental vibrations in the 5-20Hz band. If the environmental vibration level changes abruptly during the test or if the vibration level obtained from the registers below does not fall within the specified range (25,000 to typ. 500,000,000), the diagnostic result may indicate an indeterminable status or show an incorrect diagnostic result.

  To use this function, execute the **SENS_TEST** of register: MSC_CTRL [0x02(W1)], bit [12], and check the diagnostic results in register: DIAG_STAT2 [0x0C(W0)], bit [1:0] for **X_SENS_ERR**, bit [3:2] for **Y_SENS_ERR**, and bit [5:4] for **Z_SENS_ERR**. Additionally, the environmental vibration level can be checked in register: SENTST_PW [0x4D-0x56(W0)] after the test is conducted.

- **Temperature Value**

  Determine whether the temperature sensor is operating properly.

  To use this function, execute **TEMP_TEST** of register: MSC_CTRL [0x02 (W1)], bit [9], check the **TEMP_ERR** of register: DIAG_STAT1 [0x04 (W0)], bit [9] for diagnostic result.

- **Power Supply Voltage Level**

  Determine whether the power supply voltage is within 3.0 V to 3.6 V.

  To use this function, execute **VDD_TEST** of register: MSC_CTRL [0x02(W1)], bit [8], check the **VDD_ERR** of register: DIAG_STAT1 [0x04(W0)], bit [8] for diagnostic result.

- **Nonvolatile memory**

  Determine whether the Nonvolatile memory is operating properly by consistency test of data in nonvolatile memory.

  To use this function, execute **FLASH_TEST** of register: MSC_CTRL [0x02(W1)], bit [11], check the **FLASH_ERR** of register: DIAG_STAT1 [0x04(W0)], bit [2] for diagnostic result.

4.8. Threshold Detection of Accelerometer

When the acceleration value exceeds the preset threshold, an alarm is indicated.The threshold can be set for each 1 G step within the range of 0 to 10 G upper limit and - 10 G to 0 G lower limit. At the time of shipment, the upper limit + 10 G and the lower limit - 10 G are set.

The alarm threshold is set in the registers: XA_ALARM [0x47 - 0x46 (W1)], YA_ALARM [0x49 - 0x48 (W1)], ZA_ALARM [0x4B - 0x4A (W1)] and the alarm indication is registered in FLAG [0x06 (W0)], displayed in **ALARM_ERR** of bit [4:2]. Reading **ALARM_ERR** will reset the alarm display.

4.9. Structural Resonance Warning

If strong vibration is applied at the structural resonance frequency band, which is outside the measurement band (see Cantilever Resonance Frequency in Table 1.3 Sensor Specifications), the input signal is amplified excessively due to the structural resonance of the cantilever beam, and measurement cannot be performed properly. Therefore, notification is made via the structural resonance warning flag when the measurement value becomes abnormal.

The structural resonance warning notification is displayed on **EXI_ERR** in Register: FLAG [0x06(W0)], bit [7:5]. Reading **EXI_ERR** will reset the warning notification.

4.10. External Trigger Input

The external trigger input function allows the control of the sampling data measurement timing externally by inputting a pulse signal with an appropriate period to the EXT terminal. By enabling the **EXT_SEL** (MSC_CTRL [0x02(W1)], bit [7:6]), EXT pin can be used as External Trigger Input pin. The polarity of External Trigger Input (Positive Pulse / Negative Pulse) can be selected by **EXT_POL** (MSC_CTRL [0x02(W1)], bit [5]).

When this function is active, the operation is as follows:

- For UART Auto Sampling:

  When External Trigger Input pin is asserted, the latest sampling data is set to each register and sent to Host automatically.

- For all other modes:

  When External Trigger Input pin is asserted, the latest sampling data is set to each register and Data Ready signal is asserted. The Host should then read the sampling data synchronized with Data Ready signal.

Note) In case of External Trigger function usage please apply appropriate filter setting (**FILTER_SEL**) depending on the External Trigger period. Inappropriate filter setting may affect sensor noise performance.

Note) The jitter accuracy of this measurement is guaranteed except for the first sampling data from the start of the measurement and the first sampling data after the external trigger input signal is interrupted and resumed.

The External Trigger Input Timing requirements and timing diagrams are shown in Figure 4.7 and Figure 4.8.

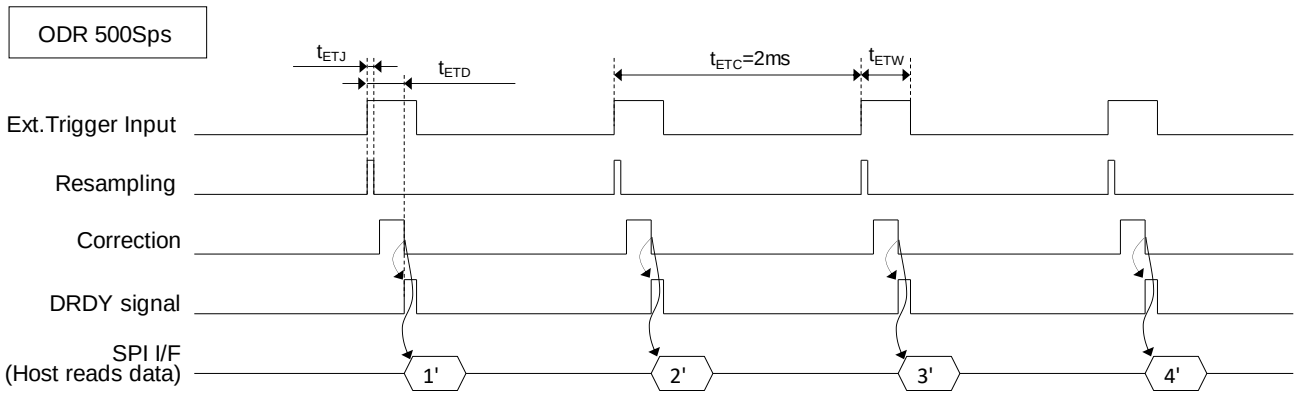


Figure 4.7 External Trigger Input (Auto Sampling)

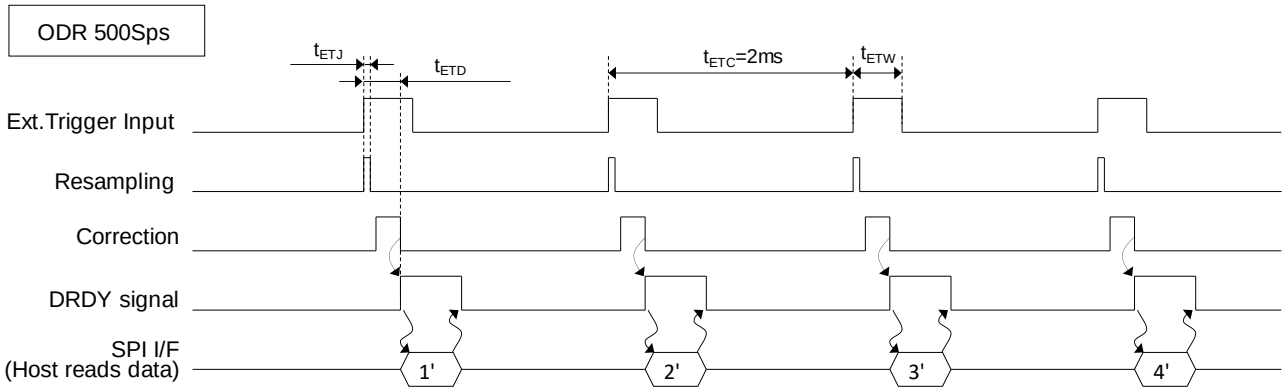


Figure 4.8 External Trigger Input (UART/SPI Manual Sampling)

4.11. 1 PPS Signal Input

The 1 PPS signal input function is intended to synchronize the sampling timing with a 1 PPS signal generated from a GNSS receiver or similar device with a holdover function by inputting the signal into the EXT terminal.

By enabling this function with **EXT_SEL** in the register: MSC_CTRL [0x02(W1)], bits [7:6], the EXT terminal can be used as a 1 PPS signal input terminal. Additionally, the polarity of the 1 PPS signal input (positive logic pulse / negative logic pulse) can be selected with **EXT_POL** in the register: MSC_CTRL [0x02(W1)], bit [5].

Figure 4.9 shows the timing and timing chart when inputting a 1 PPS signal.

Note: If a 1 PPS signal is interrupted, synchronization will be lost immediately, and no further output will be generated. To ensure stable synchronization, use a 1 PPS signal with guaranteed 1 PPS output. If the 1 PPS signal cycle deviates from tPPS ± 1 ms (typ.), a no-input notification for the 1 PPS signal will be displayed in the **1PPS_ERR** of register: FLAG [0x06(W0)], bit [8], at the end of the next 1 PPS signal cycle. This notification will also be displayed at the first 1 PPS signal input at the start of the measurement.

Note: The jitter accuracy of this measurement is guaranteed except for the first sampling data from the start of the measurement and the first sampling data after the 1 PPS signal is interrupted and resumed.

Note) For the accuracy of the 1 PPS signal input, please refer to the 1 PPS Input Cycle in Table 1.4 Interface Specifications.

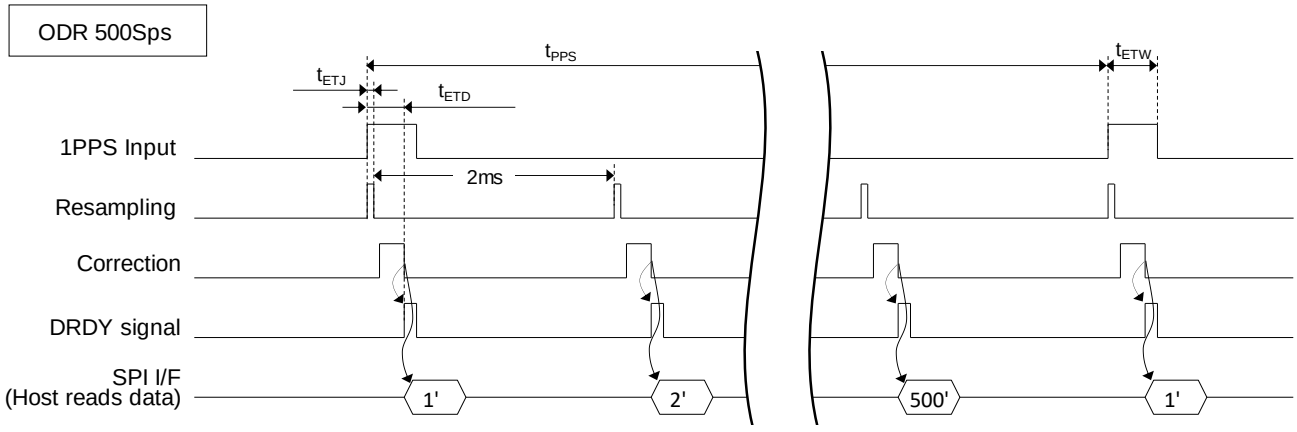


Figure 4.9 1 PPS signal input (Auto Sampling)

4.12. Checksum

A checksum can be appended to the response data during UART/SPI Burst mode or UART Auto sampling by enabling this

function in **CHKSM_OUT** (BURST_CTRL [0x0C(W1)], bit [0]).

The range of the data content for checksum is after the address byte (AD = 0x80) of the response data (Figure 4.10). The checksum is calculated with a simple addition of the data content in units of 16-bit, and the resulting sum is truncated to 16-bits and appended as checksum just before delimiter byte (CR = 0x0D).

For example:

Because the sum is "611B4" for the response data stream of "FE01 C455 4000 0052 33C0 0043 7BC8 004A 2608 FD73 3AA0 FF75 4C30 1F53 8FD0 0600 0014", the checksum is "11B4":

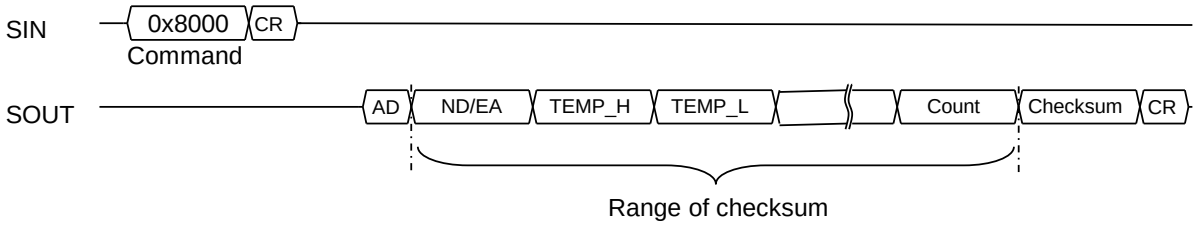


Figure 4.10 Checksum

4.13. Automatic Start (For UART Auto Sampling Only)

Automatic Start function is designed to be used in conjunction with the UART Auto sampling. When the power is supplied or the device is restart/reset, it allows the device to automatically enter Sampling mode after completing internal initialization. Please refer to Figure 4.3 for the state transition.

Follow the procedures below to enable the Automatic Start function:

- Write a “1” to both **UART_AUTO** (bit [0]) and **AUTO_START** (bit [1]) of UART_CTRL [0x08(W1)].
- Store the current register settings to non-volatile memory by writing a “1” to **FLASH_BACKUP** (GLOB_CMD [0x0A(W1)], bit [3]). After completion of the **FLASH_BACKUP** command, confirm the results by **FLASH_BU_ERR** (DIAG_STAT1 [0x04(W0)], bit [0]).
- The device will automatically enter Sampling Mode after the power supply is cycled, or a hardware reset, or a software reset command is executed.

Follow the procedures below to disable this function.

- After entering sampling mode with automatic start, write "10" to **MODE_CMD** of register: MODE_CTRL [0x02 (W0)], bit [9:8] and enter the configuration mode.
- Write "0" to **AUTO_START** of register: UART_CTRL [0x08 (W1)], bit [1].
- The subsequent steps are the same as above to store the register setting to nonvolatile memory and restart or reset the device.

4.14. Bias Offset

This function adjusts acceleration bias of X, Y, Z axis. The user specified offset is applied to the measured acceleration value before being sent out the serial interface.

Set the bias offset value to the registers: XA_OFFSET [0x2F - 0x2C (W1)], YA_OFFSET [0x33 - 0x30 (W1)], ZA_OFFSET [0x37 - 0x34 (W1)]. The adjustment range is - 10 G to + 10 G. The data format is the same as the output format of register: ACCL [0x3A - 0x30 (W0)]. Both the X, Y, and Z axes are set to "0" when shipped.

4.15. Tilt Output / Combination Output

The device can be configured to output tilt angle by register setting. The tilt angle is calculated from the measured

gravitational acceleration vector. The calculation formulas are as follows.

The device is configurable to select the measurement output type for each axis to be either acceleration or tilt angle. The measurement output type is selected with **OUTPUT_SEL** of register: SIG_CTRL [0x00 (W1)], bit [7:5].

When both acceleration and tilt angle is outputting at the same time, set **OUTPUT_SEL** to "Tilt angle" and read register: ACCL [0x3A - 0x30 (W0)] and register: TILT [0x46 - 0x3C (W0)] in normal mode.

4.16. Intermittent Measurement for Total Current Reduction

This explains how to realize intermittent measurement for reducing the device current consumption. The user can realize the intermittent measuremet by one of the methods below.

(1) Method of using a sleep mode

(2) Method of switching the device power directly on and off

Table 4.1 shows a summary of some essential items and characteristics.

Table 4.1 Summary of Intermittent Measurement Characteristics and Parameters

	(1) Using sleep mode	(2) Device power on and off
Switching method	Controlling a register and an EXT pin.	Switching the M-A352 power directly on and off
Current consumption at standby	2.2 mA Typ.	0 mA
Wakeup time	16 ms Max.	900 ms Max.
Advantage	Short wakeup time from sleep mode to sampling mode	Minimum current consumption at standby (power off)
Disadvantage	-	Necessity for design considerations to correctly handle floating device interface pins, or unpowered pins during standby mode (power off) and transition current at wakeup (power on)
Example of intended use	Event-driven measurement	Occasional measurement and long standby (power off) time

Note) When returning to sampling mode, current consumption increases from a low level to the typical current at sampling mode. This causes an increase in internal heating of the device resulting in a transitional increase in temperature compensation errors.

Note) The extent of the errors depends on many variables such as standby time, environment conditions, etc, therefore, the user should evaluate carefully these effects when used for strict and high precision measurement scenarios.

(1) Method of using sleep mode

The sleep mode function can be enabled by register setting. When shifting to sleep mode, internal circuit operation stops and current consumption during standby mode can be reduced to 2.2 mA (Typ.). Wakeup time from sleep mode to sampling mode can be shorter than that from power on to start time (reduced from 900 ms to 16 ms).

Put the operation mode from configuration mode into sleep mode by writing “11” to **MODE_CMD** (MODE_CTRL [0x02(W0)], bit [9:8]). The device can wake up from sleep mode to configuration mode in Sleep Wake-up Time by detecting an edge trigger on the EXT pin. Timing sequence from configuration mode to sleep mode and vice versa are shown in Figure 4.11.

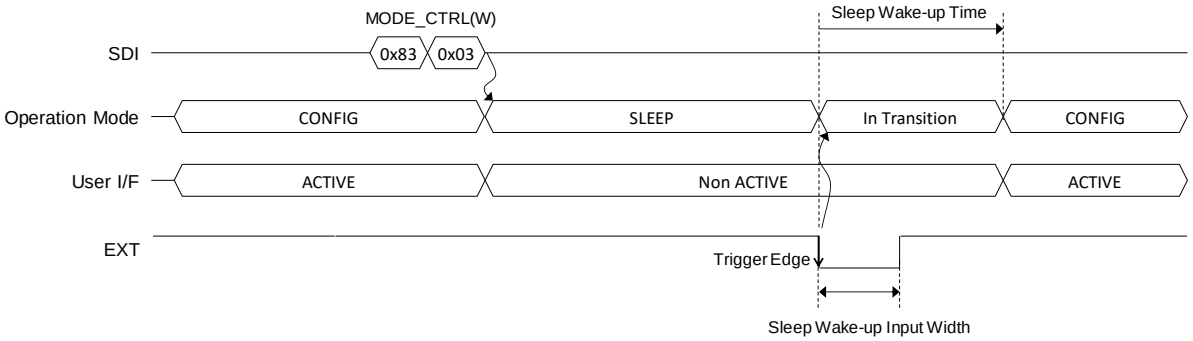


Figure 4.11 Timing Sequence from Configuration Mode to Sleep Mode and Vice Versa

(2) Method of switching the device power directly on and off

When the device power is directly switched on and off, the current consumption during standby mode can be 0 mA. Wakeup time from standby to sampling mode is exactly the same as that from power on to start time (900 ms). Please refer to “4.2 Operation Mode” for timing sequence from the power on to sampling mode.

Note) The communication interface pins shown in Table 1.6 will be un-powered during standby (the device power being off), and transition current will appear at wakeup time (device power on). The system interface to the device may need additional design considerations to mitigate the effects, i.e. an unpowered device input pin appears as a short circuit to GND to the host system or when the device is powered on before the system interface to these pins are driven (floating input).

4.17. Filter

The device has a programmable internal FIR filter. The intermediate sensor signal at 4k sps is processed by the FIR filter and decimated according to the output timing and sent out the serial interface. The number of TAPs and a cutoff frequency can be set with the FILTER_CTRL [0x06 (W1)] register.

4.17.1 FIR Kaiser Filter

Filter parameters correspond to the Kaiser window parameters.

The number of TAPs can be set to 64, 128, or 512, and the cutoff frequency Fc can be selected according to the output sample rate. Figure 4.12 to Figure 4.15 show the typical characteristic of the filters.

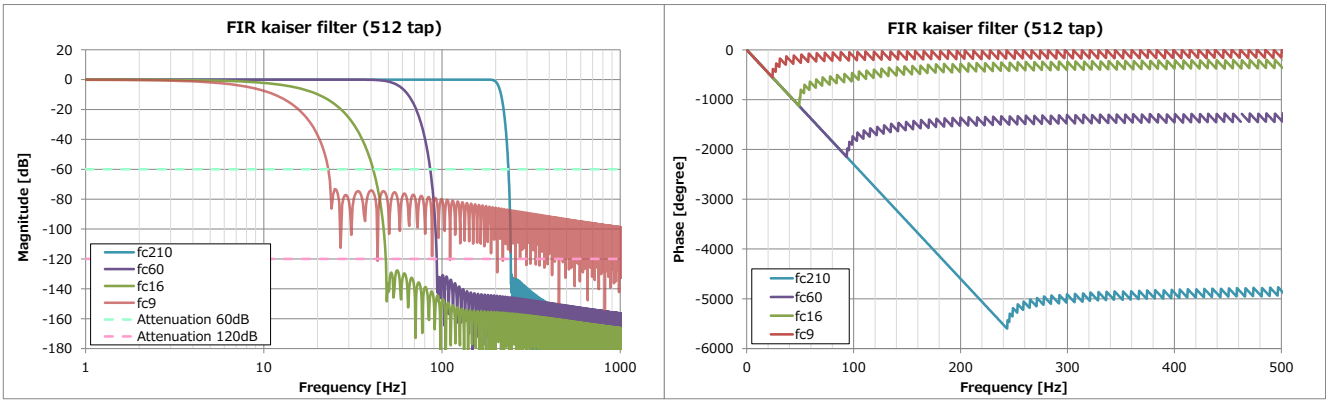


Figure 4.12 FIR Kaiser Filter Characteristic (512 taps)

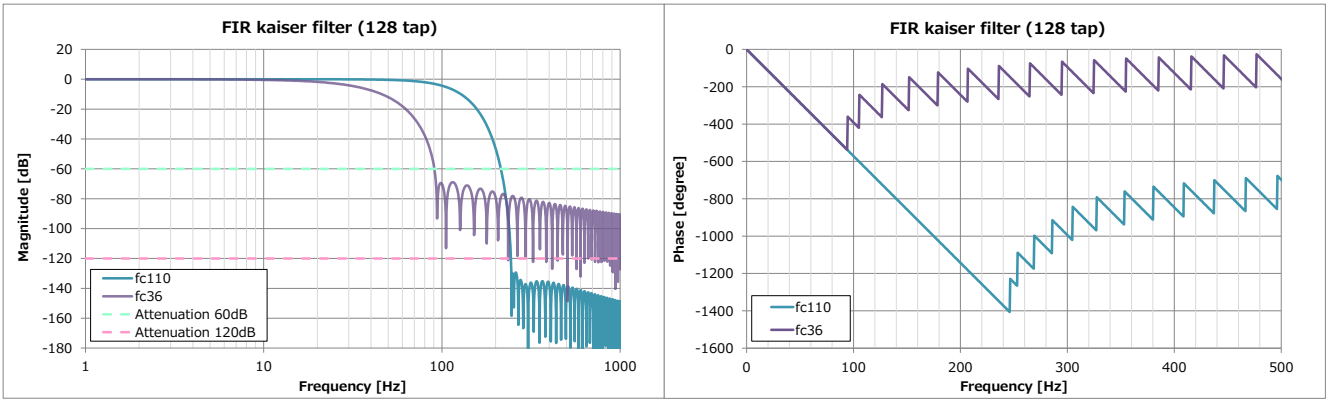


Figure 4.13 FIR Kaiser Filter Characteristic (128 taps)

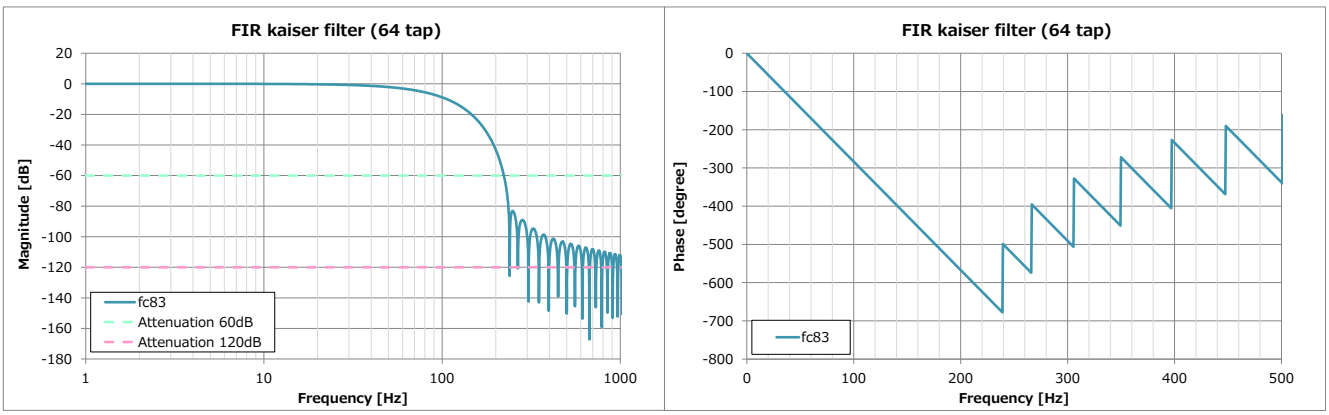


Figure 4.14 FIR Kaiser Filter Characteristic (64 taps)

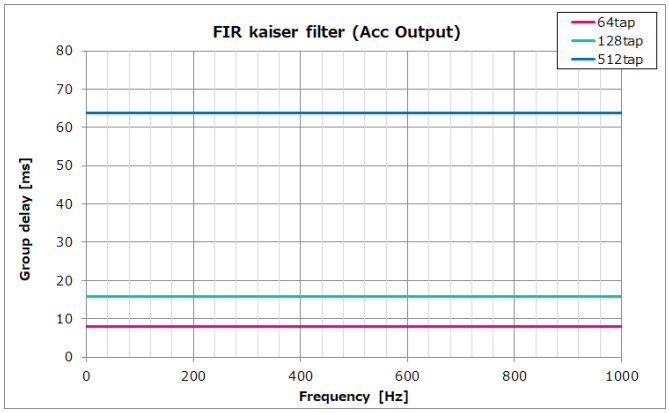


Figure 4.15 FIR Kaiser Filter Characteristic – Group Delay

4.17.2 User Defined FIR Filter

The FIR filter can be arbitrarily defined by properly setting filter coefficients in the registers: FIR_UCMD [0x16 (W1)], FIR_UDATA [0x18 (W1)], FIR_UADDR [0x1A (W1)], and set **FILTER_SEL** of register: FILTER_CTRL [0x06 (W1)] to "user defined FIR filter".

Follow the procedures below to program the user defined FIR filter.

- Register Programming Preparation

  Set the filter coefficient value using signed 32 bit fixed point number with decimal point after bit [31]. For example, if the coefficent value in decimal form is 0.2195378928, the corresponding filter coefficient value in signed 32 bit fixed point form is 0.2195378928*231 ≒ 0x1C19D153.

  Table 4.2 shows the address ranges for the filter coefficients, and Figure 4.16 shows a N-tap FIR filter architecture and a coefficient memory map. The start address is common to each tap number and is at 0x0800. No specific values are set in memory at the factory shipment.

Table 4.2 User Defined FIR Filter Coefficient Address Ranges

Tap	Coefficient Address Range
4	0x0800-0x080F
64	0x0800-0x08FF
128	0x0800-0x09FF
512	0x0800-0x0FFF

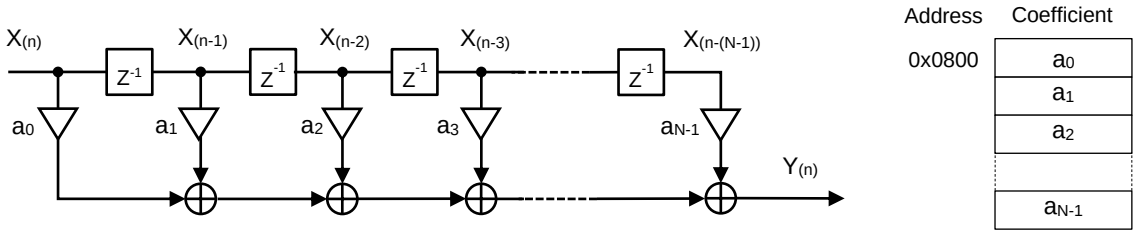


Figure 4.16 N-tap FIR Filter Architecture and Coefficient Memory Map

- Register Control (Write)

  Set the filter coefficient address in register: FIR_UADDR [0x1B, 0x1A (W1)] and set the filter coefficient value in **FIR_UDATA** of register: FIR_UDATA [0x18 (W1)].

Set **FIR_UCMD** of register: FIR_UCMD [0x16 (W1)], bit [1:0] to write the coefficient value. Next coefficient value can be set after waiting until the **FIR_UCMD** of registeris to be “00: execution complete”

After the byte has completed writing, the address is automatically incremented by 1, so continuous programming of coefficients are possible without requiring additional address settings.

For the coefficient value, set the upper byte to the upper address and the lower byte to the lower address. Figure 4.17 shows the write sequence.

Please specify the type of filter,TAP setting and cutoff frequency using **FILTER_SEL** in register: FILTER_CTRL [0x06 (W1)], bit [3:0]. When selecting the user defined FIR filter, the **FILTER_SEL** register must reflect the filter coefficient data that are programmed in the device.

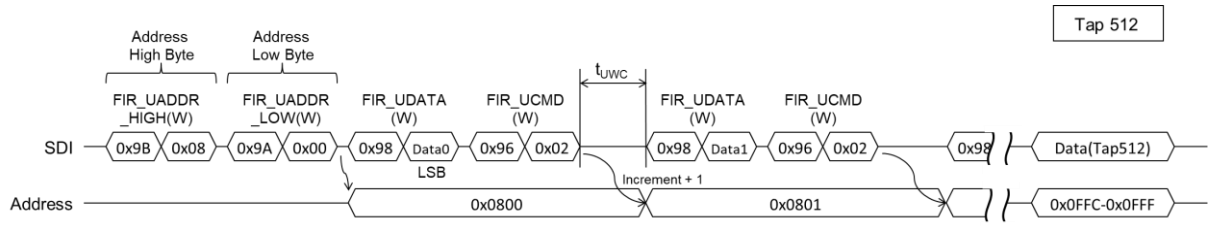


Figure 4.17 User Defined FIR Filter Coefficient Example Write Sequence (512 taps)

- Register Control (Read)

Set the filter coefficient address in register: FIR_UADDR [0x1B, 0x1A (W1)] and read the coefficient value using **FIR_UCMD** in register: FIR_UCMD [0x16 (W1)], bit [1:0]. Next coefficient value can be read after waiting until the **FIR_UCMD** of registeris to be “00: execution complete”

The address is automatically incremented by 1, so continuous execution of read commands is possible without requiring additional address settings. Figure 4.18 shows the read sequence.

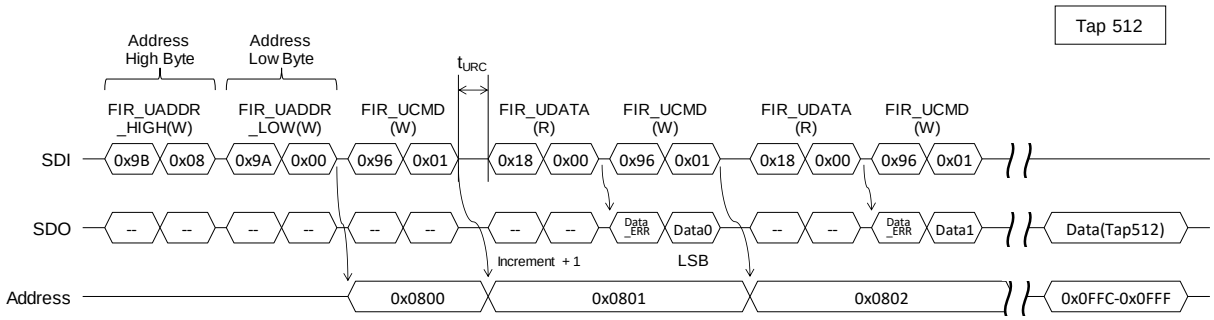


Figure 4.18 User Defined Filter Coefficient Read Sequence (512 taps)

4.17.3 Notes For FIR Filter Usage

- Transient response

As shown in Table 4.3, transient response data is generated according to the combination of the tap number and the data output rate when sampling is started.

In the case of internal timer trigger measurement, the acceleration value of register ACCL [0x3A - 0x30(W0)] is not updated during this period.

In the case of automatic measurement, the device starts outputting data after the transient response.

Table 4.3 Transient Response Data Based on Output Data Rate and Filter Tap

	64 Taps	128 Taps	512 Taps
1,000sps	15	31	127
500sps	7	15	63
200sps		7	31
100sps			15
50sps			7

- Supported Settings For Output Rate and Filter Cutoff Frequency

The host must set the cutoff frequency of the FIR filter and the output rate in proper combination to avoid aliasing.

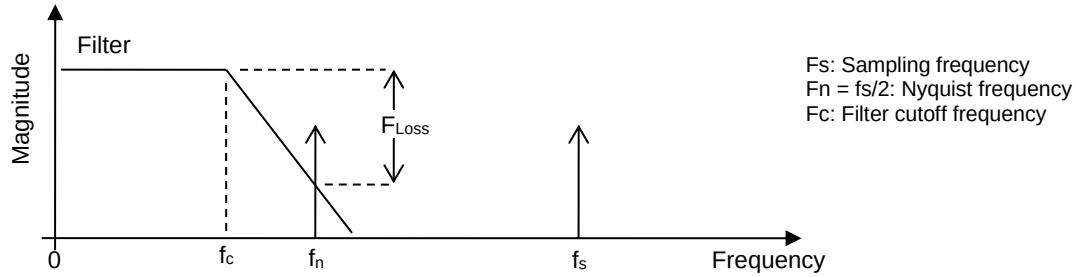


Figure 4.19 Anti-Aliasing Relationship Diagram

Table 4.4 Supported Settings For Output Rate and Filter Cutoff Frequency

				SMPL_CTRL Register (Internal Timer Trigger)				
	Tap	Fc	Group delay	Output Data Rate				
				50 Hz	100 Hz	200 Hz	500 Hz	1,000 Hz
FILTER_CTRL Register	512 tap	210 Hz	63.875 ms	-	-	-	OK	OK
		60 Hz		-	-	OK*1	OK	OK
		16 Hz		-	OK	OK	OK	OK
		9 Hz		*	*	*	*	*
	128 tap	110 Hz	15.875 ms	-	-	-	OK	OK
		36 Hz		-	-	*	*	*
	64 tap	83 Hz	7.875 ms	-	-	-	*	*

OK : F_{Loss} < -120 dB Recommended setting
* : F_{Loss} < -60 dB Although a possible setting, some decrease in measurement quality due to aliasing
\- : Fn < Fc Invalid setting. When using internal timer measurement, measurement data returns with error “0x64000000".
Note) These settings are valid when the user defined FIR filter function is used or the external trigger input function is active,

*1) The factory setting is Tap: 512, Fc: 60 Hz, ODR: 200 Hz

4.17.4 Long-Term Filter (LPF)

In addition to the FIR filter, this product has a simple filter for long-term measurement. This filter consists of a moving average at an output data rate. The number of taps can be set to a power of 2 in the range 4 to 4096.LPF is a two-stage configuration with the set number of taps.

When using a long-term filter, set **FILT_EN** of register: LONGFILT_CTRL [0x1C (W1)], bit [0] to "1: valid". Set the number of taps to **TAP_SIZE** of register: LONGFILT_TAP [0x1E (W1)].

Please note that transient response data is generated according to the tap size when sampling is started. Numbers of the transient response data for long period filters is twice the tap size.

Note) The maximum output rate is limited to 500 Sps when long-term filter is used.

5. Digital Interface

This device has the following two external interfaces.

(1) SPI interface

(2) UART interface

The SPI interface and the UART interface have almost the same functions, except for Auto sampling function for the UART interface. No hardware pin configuration is necessary for SPI/UART selection since both interfaces are always active. Connect desired interface pins to SPI or UART interface.

Note) Connecting both SPI and UART at the same time is not supported and may result in malfunction of the device.

The registers inside the device are accessed via the SPI or UART interfaces.

In this document, data sent to the device is called a “Command” and data sent back in response to the command is called a “Response”. There are two types of commands: write command and read command. The write command has no response. The write command always writes to the internal register in 8-bit words. The response to the read command, i.e. the data from the internal register, is always read in 16-bit words.

When reading from the registers, there is a burst mode in addition to the normal mode.

When the output data size is large, it may exceed the bandwidth of the host interface and cause the data transmission to be incorrect. In this case, the user must balance the transmission data rate and the bandwidth capability of the host interface.

Adjust the following settings accordingly to optimize the host interface bandwidth:

- For the UART, adjust the baud rate in **BAUD_RATE** (UART_CTRL [0x08(W1)], bit [9:8]).
- For the SPI, adjust the host side SPI clock frequency and SPI wait time.

Adjust the following settings accordingly to optimize the transmission data rate:

- The transmission data rate is affected by the data output rate setting in **DOUT_RATE** (SMPL_CTRL [0x04(W1)] bits [11:8]).
- The transmission data rate is also affected by the number of output bytes included in burst mode read transfer. The adjustment to the number of output bytes is in registers BURST_CTRL [0x0C(W1)].

Several concrete examples for setting the transmission data rate and host interface bandwidth are shown below:

(1) For UART Output:

- **BAUD_RATE** = “01" of UART_CTRL [0x08(W1)], bit [9:8]: 460800 baud
- **UART_AUTO** = “1" of UART_CTRL [0x08(W1)], bit [0]: UART Auto sampling
- **DOUT_RATE** = “0100” of SMPL_CTRL [0x04(W1)], bit [11:8]: 200 Sps
- BURST_CTRL [0x0C(W1)] = “0x4702”: TEMP, Acceleration, and COUNT output

(2) For SPI Output:

- SPI Interface Transmission Setting: fSCLK = 1 MHz and tSTALL = 24 µs for normal mode
- **DOUT_RATE** = “0100” of SMPL_CTRL [0x04(W1)], bit [11:8]: 200 Sps
- BURST_CTRL [0x0C(W1)] = “0x4702” : TEMP, Acceleration, and COUNT output

5.1. SPI Interface

Table 5.1 shows the communication settings of SPI interface and Table 5.2 shows the SPI timing for normal mode.

Table 5.1 SPI Communication Settings

Parameter	Setting
Mode	Slave
Word length	16 bits
Phase	Rising Edge
Polarity	Negative Logic

Table 5.2 SPI Timing (Normal Mode)

Parameter	Minimum	Maximum	Unit
f_{SCLK}	0.01	2.0	MHz
t_{STALL}	20	-	µs
$t_{WRITERATE}$	40	-	µs
$t_{READRATE}$	40	-	µs

5.1.1. SPI Read Timing (Normal Mode)

The response data to a read command, i.e. the data from the internal register, is always returned in 16-bit words. The SPI interface supports sending the next command during the same bus cycle as receiving a response to the read command (full-duplex).

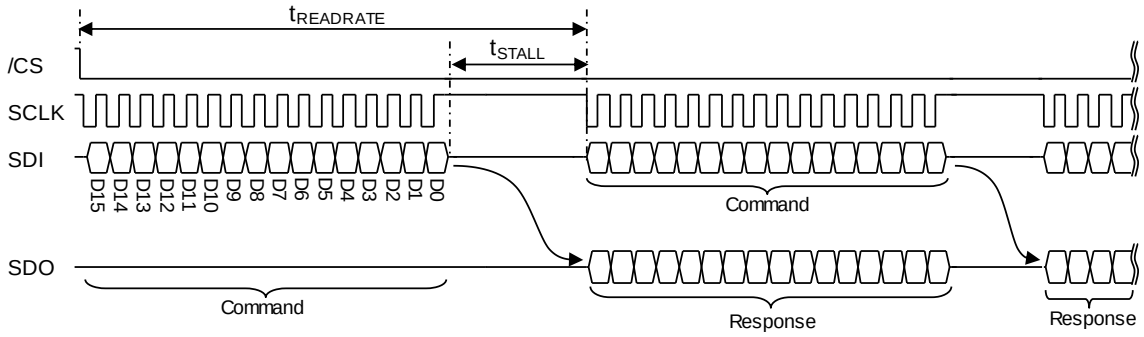


Figure 5.1 SPI Read Timing (Normal Mode)

Table 5.3 Command Format (Read)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	A [6:0]							XX							

A [6:0] ・・・ Register address (even address)
XX ・・・ Don't Care

Table 5.4 Response Format (Read)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D [15:8]								D [7:0]							

D [15:8] ・・・ Register read data (upper byte)
D [7:0] ・・・ Register read data (lower byte)

5.1.2. SPI Write Timing (Normal Mode)

A write command to a register has no response. Unlike register reading, registers are written in 8-bit words.

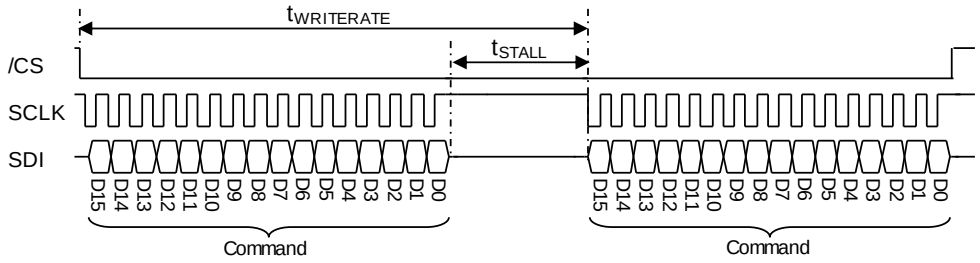


Figure 5.2 SPI Write Timing (Normal Mode)

Table 5.5 Command Format (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	A [6:0]							D [7:0]							

A [6:0] ・・・ Register address (even or odd number)
D [7:0] ・・・ Register write data

5.1.3. SPI Read Timing (Burst Mode)

Burst mode access of read data is supported using a “Burst Read Command” by writing 0x00 in **BURST_CMD** (BURST [0x00(W0)], bit [7:0]). In burst mode, ND flag/EA flag, temperature value, 3-axis acceleration value, etc. are consecutively sent as a response. The response format for the burst read output data is configured by register setting in BURST_CTRL [0x0C(W1)]. Please refer to 5.3 Data Packet Format for the response format.

Table 5.6 SPI Timing (Burst Mode)

Parameter	Minimum	Maximum	Unit
f_{SCLK}	0.01	2.0	MHz
t_{STALL1}	45	-	µs
t_{STALL2}	0	-	µs
$t_{READRATE2}$	8	-	µs

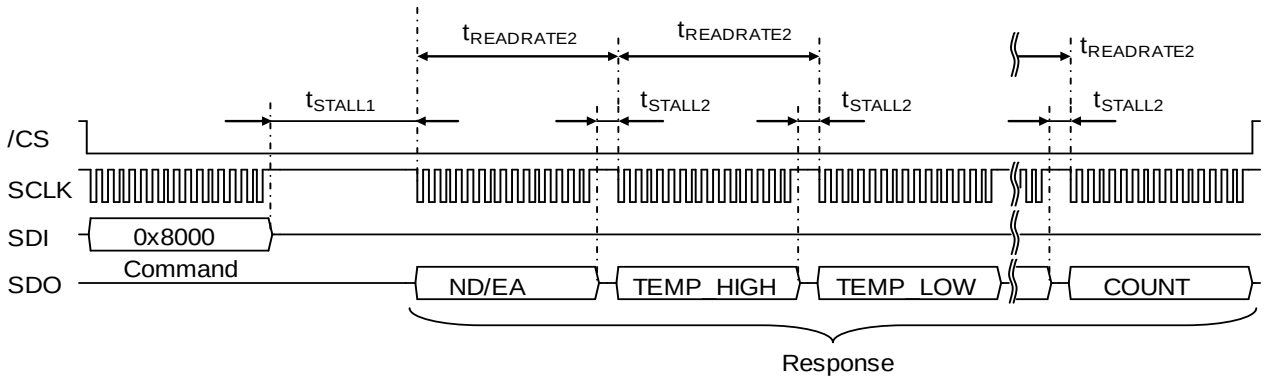


Figure 5.3 SPI Read Timing (Burst Mode)

5.2. UART Interface

Table 5.7 shows the supported UART communication settings and Figure 5.4 shows the UART bit format. Please refer to **BAUD_RATE** (UART_CTRL [0x08(W1)], bit [9:8]) for changing the baud rate setting.

Table 5.7 UART Communication Settings

Parameter	Settings
Transfer rate	115.2 kbps / 230.4 kbps / 460.8 kbps
Start	1 bit
Data	8 bits
Stop	1 bit
Parity	None
Delimiter	CR (0x0D)

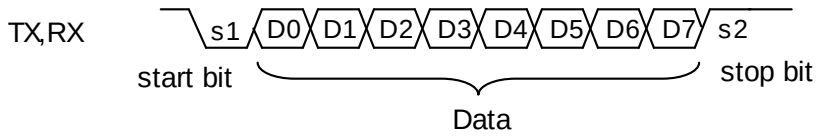


Figure 5.4 UART Bit Format

For the UART interface, a delimiter (1 byte) is placed at the end of each command (by the host) and response (by this device). In addition for responses, the address (1 byte) specified by the command is added (by this device) to the beginning of the response.

Table 5.8 and Table 5.9 shows the timing of UART.

Table 5.8 UART Timing

Parameter	Normal Mode		Manual Sampling Burst Mode		Auto Sampling Auto Mode		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	
t_{STALL}	-	25	-	45	-	- *2	µs
$t_{WRITERATE}$ (115.2 kbps)	660	-	-	-	660	-	µs
$t_{WRITERATE}$ (230.4 kbps)	350	-	-	-	350	-	µs
$t_{WRITERATE}$ (460.8 kbps)	200	-	-	-	200	-	µs
$t_{READRATE}$ (115.2 kbps)	660	-	*1	-	- *2	-	µs
$t_{READRATE}$ (230.4 kbps)	350	-	*1	-	- *2	-	µs
$t_{READRATE}$ (460.8 kbps)	200	-	*1	-	- *2	-	µs

*1) Please refer to Table 5.9.

*2) Register reading is not supported while in Sampling Mode with UART Auto Sampling enabled.

Table 5.9 UART Timing ($t_{READRATE}$ requirements for Burst Mode)

Parameter	Burst Mode (Min.)	Unit
$t_{READRATE}$ (115.2 kbps)	660 + 86.8 × B	µs
$t_{READRATE}$ (230.4 kbps)	350 + 43.4 × B	µs
$t_{READRATE}$ (460.8 kbps)	200 + 21.7 × B	µs

B = Number of receive data bytes (AD: address and CR: delimiter is not included).

Example tREADRATE Calculation:

BURST_CTRL [0x0C(W1)]: Set value 0x4702

B = 18 byte for the above stated register setting

$t_{READRATE}$ (460.8 kbps) = 200 + (21.7 × 18) = 591 (µs)

5.2.1. UART Read Timing (Normal Mode)

The response to the read command, i.e. the data from the internal register, is always returned 16-bit data at a time. The register address (AD) comes at the beginning of the response, for example, 0x02 for the MODE_CTRL [0x02(W0)] register.

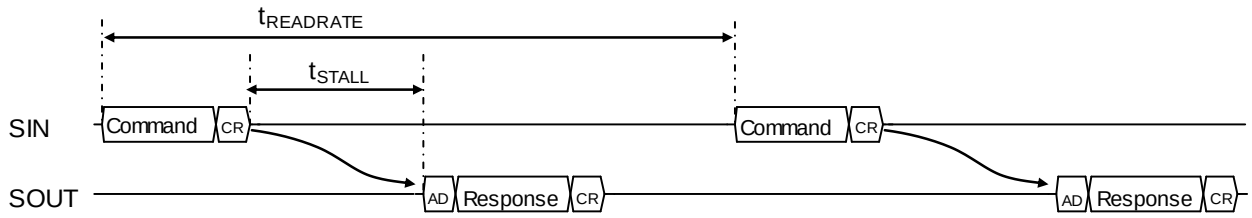


Figure 5.5 UART Read Timing (Normal Mode)

Table 5.10 Command Format (Read)

The first byte								The second byte								The third byte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	A [6:0]							XX								0x0D							

A [6:0] ・・・ Register address (even address)
XX ・・・ Don't Care
0x0D ・・・ Delimiter

Table 5.11 Response Format (Read)

The first byte								The second byte								The third byte								The fourth byte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	A [6:0]							D [15:8]								D [7:0]								0x0D							

A [6:0] ・・・ Register address (even address)
D [15:8] ・・・ Register read data (upper byte)
D [7:0] ・・・ Register read data (lower byte)
0x0D ・・・ Delimiter

5.2.2. UART Read Timing (Burst Mode)

Burst mode access of read data is supported using a “Burst Read Command” by writing 0x00 in **BURST_CMD** (BURST [0x00(W0)], bit [7:0]). In Burst Mode, ND/EA flag, temperature value, 3-axis acceleration value, etc. are consecutively sent as a response. The response format for the burst read output data is configured by register setting in BURST_CTRL [0x0C(W1)]. Please refer to 5.3 Data Packet Format for the response format.

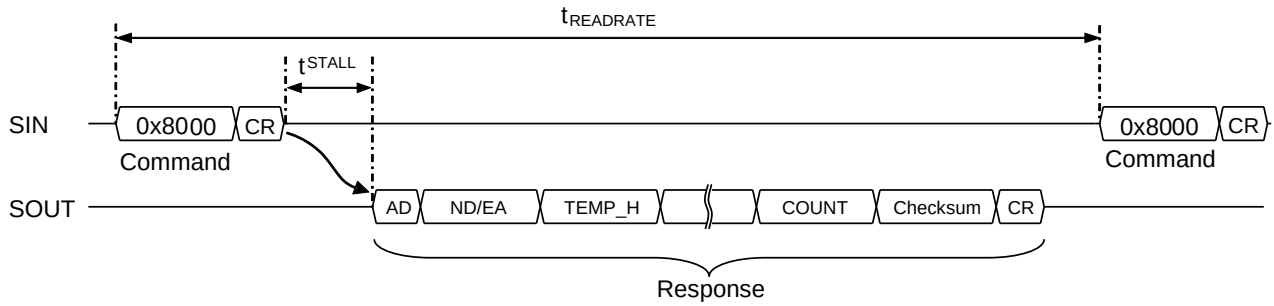


Figure 5.6 UART Read Timing (Burst Mode)

Table 5.12 Command Format (Burst Mode)

The first byte								The second byte								The third byte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0x80								0x00								0x0D							

0x80 ・・・ Burst Command
0x00 ・・・ Burst Data 0x00
0x0D ・・・ Delimiter

5.2.3. UART Write Timing

A write command to a register will have no response. Unlike register reading, registers are written in 8-bit words.

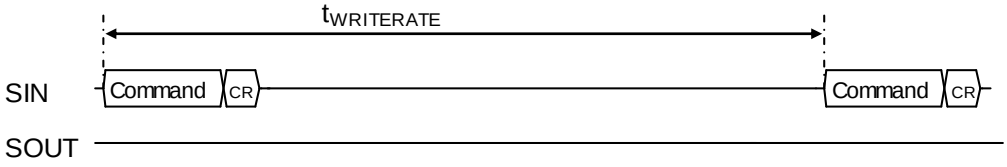


Figure 5.7 UART Write Timing

Table 5.13 Command Format (Write)

The first byte								The second byte								The third byte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	A [6:0]							D [7:0]								0x0D							

A [6:0] ・・・ Register address (even or odd number)
D [7:0] ・・・ Register write data
0x0D ・・・ Delimiter

5.2.4. UART Auto Sampling Operation

When UART Auto sampling is active, all sensor outputs are sent as burst transfer automatically at the programmed output data rate without the request from the Host. For information about the response format, see 5.3 UART Data Packet Format. The response format for the burst read output data is configured by register setting in BURST_CTRL [0x0C(W1)].

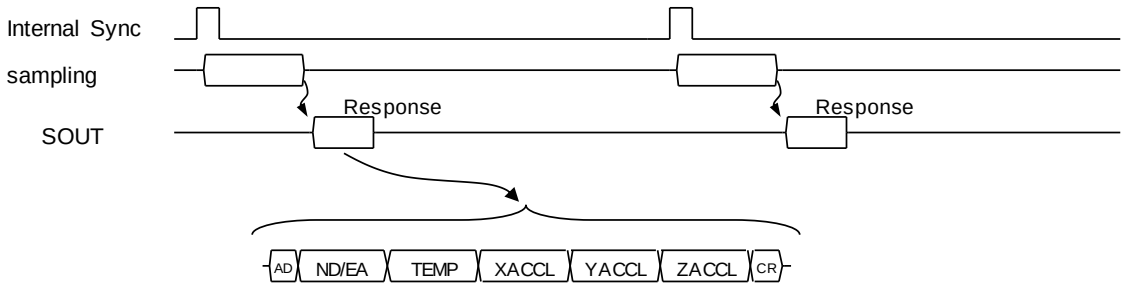


Figure 5.8 UART Auto Sampling

5.3. Data Packet Format

The following table shows example of the data packet format sent to the host in the UART Burst Mode or UART Auto Sampling and SPI burst mode.

Table 5.14 Example of Data Packet Format 1 (UART BURST / AUTO SAMPLING)

BURST_CTRL [0x0C(W1)] = 0xC703 (Burst Output: Flag, Temp, Acceleration, Counter, Checksum)
SIG_CTRL [0x00(W1)] = 0x8E00 (Output Mode: Acceleration)

Byte No.	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	ADDRESS	0x80							
2	ND	ND (Temp)	-	-	-	ND (XACCL)	ND (YACCL)	ND (ZACCL)	1PPS ERR
3	EA	X_EXI ERR	Y_EXI ERR	Z_EXI ERR	XALARM ERR	YALARM ERR	ZALARM ERR	ALIASI ERR	EA
4	TEMP_HIGH_H	TEMP_HIGH [15:8]							
5	TEMP_HIGH_L	TEMP_HIGH [7:0]							
6	TEMP_LOW_H	TEMP_LOW [15:8]							
7	TEMP_LOW_L	TEMP_LOW [7:0]							
8	XACCL_HIGH_H	XACCL_HIGH [15:8]							
9	XACCL_HIGH_L	XACCL _HIGH [7:0]							
10	XACCL_LOW_H	XACCL_LOW [15:8]							
11	XACCL_LOW_L	XACCL _LOW [7:0]							
12	YACCL_HIGH_H	YACCL _HIGH [15:8]							
13	YACCL_HIGH_L	YACCL _HIGH [7:0]							
14	YACCL_LOW_H	YACCL _LOW [15:8]							
15	YACCL_LOW_L	YACCL _LOW [7:0]							
16	ZACCL_HIGH_H	ZACCL _HIGH [15:8]							
17	ZACCL_HIGH_L	ZACCL _HIGH [7:0]							
18	ZACCL_LOW_H	ZACCL _LOW [15:8]							
19	ZACCL_LOW_L	ZACCL _LOW [7:0]							
20	COUNT_H	COUNT [15:8]							
21	COUNT_L	COUNT [7:0]							
22	CHECKSUM_H	CHECKSUM [15:8]							
23	CHECKSUM_L	CHECKSUM [7:0]							
24	CR	0x0D							

Table 5.15 Example of Data Packet Format 2 (UART BURST / AUTO SAMPLING)

BURST_CTRL [0x0C(W1)] = 0x4702 (Burst Output: Temp, Acceleration, Counter)
SIG_CTRL [0x00(W1)] = 0x8E00 (Output Mode: Acceleration)

Byte No.	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	ADRESS	0x80							
2	TEMP_HIGH_H	TEMP_HIGH [15:8]							
3	TEMP_HIGH_L	TEMP_HIGH [7:0]							
4	TEMP_LOW_H	TEMP_LOW [15:8]							
5	TEMP_LOW_L	TEMP_LOW [7:0]							
6	XACCL_HIGH_H	XACCL_HIGH [15:8]							
7	XACCL_HIGH_L	XACCL _HIGH [7:0]							
8	XACCL_LOW_H	XACCL_LOW [15:8]							
9	XACCL_LOW_L	XACCL _LOW [7:0]							
10	YACCL_HIGH_H	YACCL _HIGH [15:8]							
11	YACCL_HIGH_L	YACCL _HIGH [7:0]							
12	YACCL_LOW_H	YACCL _LOW [15:8]							
13	YACCL_LOW_L	YACCL _LOW [7:0]							
14	ZACCL_HIGH_H	ZACCL _HIGH [15:8]							
15	ZACCL_HIGH_L	ZACCL _HIGH [7:0]							
16	ZACCL_LOW_H	ZACCL _LOW [15:8]							
17	ZACCL_LOW_L	ZACCL _LOW [7:0]							
18	COUNT_H	COUNT [15:8]							
19	COUNT_L	COUNT [7:0]							
20	CR	0x0D							

Table 5.16 Example of Data Packet Format 3 (SPI BURST MODE)

BURST_CTRL [0x0C(W1)] = 0xC703 (Burst Output: Flag, Temp, Acceleration, Counter, Checksum)
SIG_CTRL [0x00(W1)] = 0x8E00 (Output Mode: Acceleration)

Word No.	Bit15	…	Bit0
1	FLAG(ND/EA)		
2	TEMP_HIGH		
3	TEMP_LOW		
4	XACCL_HIGH		
5	XACCL_LOW		
6	YACCL _HIGH		
7	YACCL _LOW		
8	ZACCL _HIGH		
9	ZACCL _LOW		
10	COUNT		
11	CHECKSUM		

Table 5.17 Example of Data Packet Format 4 (SPI BURST MODE)

BURST_CTRL [0x0C(W1)] = 0x4702 (Burst Output: Temp, Acceleration, Counter)
SIG_CTRL [0x00(W1)] = 0x8E00 (Output Mode: Acceleration)

Word No.	Bit15	…	Bit0
1	TEMP_HIGH		
2	TEMP_LOW		
3	XACCL_HIGH		
4	XACCL_LOW		
5	YACCL _HIGH		
6	YACCL _LOW		
7	ZACCL _HIGH		
8	ZACCL _LOW		
9	COUNT		

6. User Register

A host device (for example, a microcontroller) can control the device by accessing the control registers inside the device.

The registers are accessed in this device using a WINDOW method. The prescribed window number is first written to **WINDOW_ID** of WIN_CTRL [0x7E(W0/W1)], bit [7:0], then the desired register address can be accessed. The WIN_CTRL [0x7E(W0/W1)] register can always be accessed without needing to set the window number.

During the Power-On Start-Up Time or the Reset Recovery time specified in the Table 1.4 Interface Specifications, all the register values are undefined because internal initialization is in progress. Ensure the device registers are only accessed after the Power-On Start-Up Time or the Reset Recovery time is over.

For information about the initial values of the control registers after internal initialization is finished, see the "Default" column in the Table 6.1. The control registers with ○ mark in the "Flash Backup" column can be saved to the non-volatile memory by the user, and the initial values after the power on will be the values read from the non-volatile memory. If the read out from the non-volatile memory fails, the **FLASH_ERR** (DIAG_STAT1 [0x04(W0)], bit [2]) is set to 1 (error).

Please ensure that the device is in the Configuration Mode before writing to registers. In the Sampling Mode, writing to registers is ignored except for the following cases.

- **MODE_CMD** in MODE_CTRL [0x02(W0)], bit [9:8]
- **SOFT_RST** in GLOB_CMD [0x0A(W1)], bit [7]
- **WINDOW_ID** in WIN_CTRL [0x7E(W0/W1)], bit [7:0]

While in the UART Auto Mode with Sampling Mode is active, register read access is not supported. Otherwise, the sampling data transmitted in the UART Auto Mode will be corrupted by the response data from the register read.

Each register is 16-bit wide and one address is assigned to every 8 bits. Registers are read in 16-bit words and are written in 8-bit words. The byte order of each 16-bit register is little endian, but the byte order of the 16-bit data transferred over the digital interface is big endian.

Table 6.1 shows the register map, and Section 6.1 through Section 6.32 describes the registers in detail.

The "-" sign in the register assignment table in Section 6.1 through Section 6.32 means "reserved".
Write a "0" to reserved bits during a write operation.
During a read operation, a reserved bit can return either 0 or 1 ("don't care").
Writing to a read-only register is prohibited.

Note) The explanation of the register notation MODE_CTRL [0x02(W0)], bit [9:8] is as follows:

- MODE_CTRL: Register name
- [0x02(W0)]: First number is the Register Address, (W0) means Window Number "0"
- bit [9:8]: Bits 9 to 8

Table 6.1 Register Map

Name	Window ID	Address	(*3)Read Command 16bit Read	Write Command 8bitWrite	R/W	Flash Backup	Default	Function
BURST	0	0x00	-	0x80	W	-	-	Burst mode
		0x01		-	-		-	
MODE_CTRL	0	0x02	0x02XX	-	-	-	0x00	Operation mode control
		0x03		0x83	R/W		0x04	
DIAG_STAT1	0	0x04	0x04XX	-	R	-	0x00	Diagnostic result 1
		0x05		-	R		0x00	
FLAG	0	0x06	0x06XX	-	R	-	0x00	ND/EA flag
		0x07		-	R		0x00	
COUNT	0	0x0A	0x0AXX	-	R	-	0x00	Sampling count
		0x0B		-	R		0x00	
DIAG_STAT2	0	0x0C	0x0CXX	-	R	-	0x00	Diagnostic result 2
		0x0D		-	R		0x00	
TEMP_HIGH	0	0x0E	0x0EXX	-	R	-	0xFF	Temperature sensor value High
		0x0F		-	R		0xFF	
TEMP_LOW	0	0x10	0x10XX	-	R	-	0xFF	Temperature sensor value Low
		0x11		-	R		0xFF	
XACCL_HIGH	0	0x30	0x30XX	-	R	-	0xFF	X acceleration sensor value High
		0x31		-	R		0xFF	
XACCL_LOW	0	0x32	0x32XX	-	R	-	0xFF	X acceleration sensor value Low
		0x33		-	R		0xFF	
YACCL_HIGH	0	0x34	0x34XX	-	R	-	0xFF	Y acceleration sensor value High
		0x35		-	R		0xFF	
YACCL_LOW	0	0x36	0x36XX	-	R	-	0xFF	Y acceleration sensor value Low
		0x37		-	R		0xFF	
ZACCL_HIGH	0	0x38	0x38XX	-	R	-	0xFF	Z acceleration sensor value High
		0x39		-	R		0xFF	
ZACCL_LOW	0	0x3A	0x3AXX	-	R	-	0xFF	Z acceleration sensor value Low
		0x3B		-	R		0xFF	
XTILT_HIGH	0	0x3C	0x3CXX	-	R	-	0xFF	X Tilt sensor value High
		0x3D		-	R		0xFF	
XTILT_LOW	0	0x3E	0x3EXX	-	R	-	0xFF	X Tilt sensor value Low
		0x3F		-	R		0xFF	
YTILT_HIGH	0	0x40	0x40XX	-	R	-	0xFF	Y Tilt sensor value High
		0x41		-	R		0xFF	
YTILT_LOW	0	0x42	0x42XX	-	R	-	0xFF	Y Tilt sensor value Low
		0x43		-	R		0xFF	
ZTILT_HIGH	0	0x44	0x44XX	-	R	-	0xFF	Z Tilt sensor value High
		0x45		-	R		0xFF	
ZTILT_LOW	0	0x46	0x46XX	-	R	-	0xFF	Z Tilt sensor value Low
		0x47		-	R		0xFF	
SENTST_PW_X_H	0	0x50	0x50XX	-	R	-	0xFF	X sensitivity test vibration level High
		0x51		-	R		0xFF	
SENTST_PW_X_L	0	0x52	0x52XX	-	R	-	0xFF	X sensitivity test vibration level Low
		0x53		-	R		0xFF	
SENTST_PW_Y_H	0	0x54	0x54XX	-	R	-	0xFF	Y sensitivity test vibration level High
		0x55		-	R		0xFF	
SENTST_PW_Y_L	0	0x56	0x56XX	-	R	-	0xFF	Y sensitivity test vibration level Low
		0x57		-	R		0xFF	
SENTST_PW_Z_H	0	0x58	0x58XX	-	R	-	0xFF	Z sensitivity test vibration level High
		0x59		-	R		0xFF	
SENTST_PW_Z_L	0	0x5A	0x5AXX	-	R	-	0xFF	Z sensitivity test vibration level Low
		0x5B		-	R		0xFF	
SIG_CTRL	1	0x00	0x00XX	0x80	R/W	○	0x00	DataReady signal & polarity control
		0x01		0x81	R/W		0x8E	
MSC_CTRL	1	0x02	0x02XX	0x82	R/W	○	0x26	Other control
		0x03		0x83	R/W		0x00	
SMPL_CTRL	1	0x04	0x04XX	-	-	○	0x00	Sampling control
		0x05		0x85	R/W		0x04	

FILTER_CTRL	1	0x06 0x07	0x06XX	0x86 -	R/W -	○	0x08 0x00	Filter control
UART_CTRL	1	0x08 0x09	0x08XX	0x88 0x89	R/W R/W	○	0x00 0x01	UART control
GLOB_CMD	1	0x0A 0x0B	0x0AXX	0x8A -	R/W R	-	0x00 0x00	System control
BURST_CTRL	1	0x0C 0x0D	0x0CXX	0x8C 0x8D	R/W R/W	○	0x02 0x47	Burst control
FIR_UCMD	1	0x16 0x17	0x16XX	0x96 -	R/W -	-	0x00 0x00	User FIR Filter control
FIR_UDATA	1	0x18 0x19	0x18XX	0x98 -	R/W R	-	0x00 0x00	User FIR Filter coefficient data
FIR_UADDR	1	0x1A 0x1B	0x1AXX	0x9A 0x9B	R/W R/W	-	0x00 0x08	User FIR Filter coefficient Address
LONGFILT_CTRL	1	0x1C 0x1D	0x1CXX	0x9C -	R/W -	○	0x00 0x00	Long period filter control
LONGFILT_TAP	1	0x1E 0x1F	0x1EXX	0x9E -	R/W -	○	0x0A 0x00	Long period filter tap number
OFFSET_XA_HIGH	1	0x2C 0x2D	0x2CXX	0xAC 0xAD	R/W R/W	○	0x00 0x00	X acceleration offset value High
OFFSET_XA_LOW	1	0x2E 0x2F	0x2EXX	0xAE 0xAF	R/W R/W	○	0x00 0x00	X acceleration offset value Low
OFFSET_YA_HIGH	1	0x30 0x31	0x30XX	0xB0 0xB1	R/W R/W	○	0x00 0x00	Y acceleration offset value High
OFFSET_YA_LOW	1	0x32 0x33	0x32XX	0xB2 0xB3	R/W R/W	○	0x00 0x00	Y acceleration offset value Low
OFFSET_ZA_HIGH	1	0x34 0x35	0x34XX	0xB4 0xB5	R/W R/W	○	0x00 0x00	Z acceleration offset value High
OFFSET_ZA_LOW	1	0x36 0x37	0x36XX	0xB6 0xB7	R/W R/W	○	0x00 0x00	Z acceleration offset value Low
XALARM	1	0x46 0x47	0x46XX	0xC6 0xC7	R/W R/W	○	0xF6 0x0A	X acceleration alarm
YALARM	1	0x48 0x49	0x48XX	0xC8 0xC9	R/W R/W	○	0xF6 0x0A	Y acceleration alarm
ZALARM	1	0x4A 0x4B	0x4AXX	0xCA 0xCB	R/W R/W	○	0xF6 0x0A	Z acceleration alarm
PROD_ID1	1	0x6A 0x6B	0x6AXX	- -	R R	-	0x41 0x33	Product ID 1
PROD_ID2	1	0x6C 0x6D	0x6CXX	- -	R R	-	0x37 0x30	Product ID 2
PROD_ID3	1	0x6E 0x6F	0x6EXX	- -	R R	-	0x41 0x44	Product ID 3
PROD_ID4	1	0x70 0x71	0x70XX	- -	R R	-	0x31 0x30	Product ID 4
VERSION	1	0x72 0x73	0x72XX	- -	R R	-	(*1)	Firmware version
SERIAL_NUM1	1	0x74 0x75	0x74XX	- -	R R	-	(*2)	Serial Number 1
SERIAL_NUM2	1	0x76 0x77	0x76XX	- -	R R	-		Serial Number 2
SERIAL_NUM3	1	0x78 0x79	0x78XX	- -	R R	-		Serial Number 3
SERIAL_NUM4	1	0x7A 0x7B	0x7AXX	- -	R R	-		Serial Number 4
WIN_CTRL	0,1	0x7E 0x7F	0x7EXX	0xFE -	R/W -	-	0x00 0x00	Register Window Control

* 1) This depends on the version of the installed firmware.
* 2) This is determined by each individual serial number.
* 3) Lower byte XX: Do not care

6.1. BURST Register (Window 0)

Addr (Hex)	Bit15	…	Bit8	R/W
0x01	-			-

Addr (Hex)	Bit7	…	Bit0	R/W
0x00	BURST_CMD			W

bit [7:0] BURST_CMD

A burst mode read operation is initiated by writing 0x00 in **BURST_CMD** of this register.

Note) The data transmission format is described in 5.1.3 SPI Read Timing (Burst Mode) and 5.2.2 UART Read Timing (Burst Mode). Also refer to 5.3 Data Packet Format. The output data can be selected by setting BURST_CTRL [0x0C(W1)].

6.2. MODE_CTRL Register (Window 0)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x03	-	-	-	-	MODE_STAT		MODE_CMD		R/W *1

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x02	-	-	-	-	-	-	-	-	-

*1) **MODE_STAT** is read-only.

bit [11:10] MODE_STAT

This read-only status bit shows the current operation mode.
00: Sampling Mode
01: Configuration mode
10: Sleep Mode
11: (Not Used)

bit [9:8] MODE_CMD

Executes commands related to the operation mode.
00: Execute Complete.
01: Go to the Sampling Mode.
After the mode transition is completed, the bits automatically goes back to “00”.
10: Go to the Configuration Mode.
After the mode transition is completed, the bits automatically goes back to “00”.
11: Go to the Sleep Mode.
After the mode transition is completed, the bits automatically goes back to “00”.

Note) The UART and SPI interfaces cannot be used during sleep mode. To wake up from sleep mode, input an edge trigger to the EXT pin. The internal circuits of the device will recover to nomal operation by the EXT trigger, and operation state will return from sleep mode to configuration mode.

6.3. DIAG_STAT1 Register (Window 0)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x05	ACC_VEC _ERR	ACC_X _ERR	ACC_Y _ERR	ACC_Z _ERR	-	-	TEMP _ERR	VDD _ERR	R

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x04	HARD _ERR			SPI _OVF	UART _OVF	FLASH _ERR	ACC_ERR _ALL	FLASH_ BU_ERR	R

Note) When the host reads the diagnosis result, all the results (including the EA flag in the FLAG register) will be cleared to 0.

bit [15] ACC_VEC_ERR (ACC VECtor magnitude ERRor)
Shows the execution result of vector magnitude value of acceleration three axes in **ACC_TEST** of MSC_CTRL [0x02 (W1)], bit [10].
1: Error occurred
0: No error
If this error occurs, sensor is faulty.

bit [14] ACC_X_ERR
Shows the result of X axis sensor operation check in **ACC_TEST** of MSC_CTRL [0x02 (W1)], bit [10].
1: Error occurred
0: No error
If this error occurs, X axis sensor is faulty.

bit [13] ACC_Y_ERR
Shows the result of Y axis sensor operation check in **ACC_TEST** of MSC_CTRL [0x02 (W1)], bit [10].
1: Error occurred
0: No error
If this error occurs, Y axis sensor is faulty.

bit [12] ACC_Z_ERR
Shows the result of Z axis sensor operation check in **ACC_TEST** of MSC_CTRL [0x02 (W1)], bit [10].
1: Error occurred
0: No error
If this error occurs, Z axis sensor is faulty.

bit [9] TEMP_ERR
Shows the execution result of **TEMP_TEST** (Temp Sensor Check) of MSC_CTRL [0x02 (W1)], bit [9].
1: Error occurred
0: No error
If this error occurs, temperature sensor is faulty.

bit [8] VDD_ERR
Shows the execution result of **VDD_TEST** (Power Supply Voltage Check) of MSC_CTRL [0x02 (W1)], bit [8].
1: Error occurred
0: No error
If this error occurs, Check whether the power supply voltage level is within the specified range.

bit [7:5] HARD_ERR
Shows the result of the hardware check at startup.
Other than 000: Error occurred
000: No error
When this error occurs, it indicates the device is faulty.

bit [4] SPI_OVF (SPI OVer Flow)
Shows an error occurred if the device received too many commands from the SPI interface in short period of time.
1: Error occurred
0: No error
When this error occurrs, review the SPI command transmission interval and the SPI clock setting.

bit [3] UART_OVF (UART OVer Flow)
Shows an error occurred if the data transmission rate is faster than the UART baud rate.
1: Error occurred
0: No error
When this error occurs, review the settings for the baud rate (register: UART_CTRL [0x08(W1)], bit [9:8]), data output rate (register: SMPL_CTRL [0x04(W1)], bit [11:8]), UART Burst Mode / Auto sampling (register: BURST_CTRL [0x0C(W1)]) in combination.

bit [2] FLASH_ERR
Shows the result of **FLASH_TEST** of MSC_CTRL [0x02(W1)], bit [11].
1: Error occurred

0: No error
This error indicates a failure occurred when reading data out from the non-volatile memory.

bit [1] ACC_ERR_ALL (ACCTest ERRor All)
Shows the logical sum of bit [15:12] of this register.
1: Error occurred
0: No error

bit [0] FLASH_BU_ERR (FLASH BackUp ERRor)
Shows the result of **FLASH_BACKUP** of GLOB_CMD [0x0A(W1)], bit [3].
1: Error occurred
0: No error

6.4. FLAG (ND/EA) Register (Window 0)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x07	ND (Temp)	-	-	-	ND (XACCL) (XTILT)	ND (YACCL) (YTILT)	ND (ZACCL) (ZTILT)	1PPS _ERR	R

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x06	X_EXI _ERR	Y_EXI _ERR	Z_EXI _ERR	XALARM _ERR	YALARM _ERR	ZALARM _ERR	ALIASI _ERR	EA	R

Note) **EXI_ERR** flags and **ALARM_ERR** flags are cleared to "0" by reading this register. Note that in Burst mode and UART Auto sampling, these flags are cleared to "0" after every sample output regardless of the **FLAG_OUT** setting in regster BURST_CTRL, bit [15].

Note) **EA** flag is cleared to "0" by reading the DIAG_STAT1 register.

Note) The ALIASI_ERR flag is updated when writing to the SMPL_CTRL or FILTER_CTRL register.

bit [15] ND (New Data) flag (Temperature)
When new measurement data is set in temperature register: TEMP_HIGH [0x0E (W0)], this bit is set to "1". This bit is reset to “0” reading by the temperature register.

bit [11:9] ND (New Data) flag (Acceleration)
When new measurement data is set in acceleration register: XACCL_HIGH [0x30(W0)], YACCL_HIGH [0x34(W0)], ZACCL_HIGH [0x38(W0)], this bit is set to "1". This bit is reset to “0” by reading the temperature register.

bit [8] 1PPS_ERR
Displays when no 1 PPS signal is input in 1 PPS measurement mode.
1: No 1 PPS signal input
0: 1 PPS signal input present

bit [7] X_EXI_ERR
This bit indicates when the measured value of X-axis becomes abnormal due to structural resonance in the sensor.
1: Measurement value is abnormal due to structural resonance
0: Measured value is within normal range

bit [6] Y_EXI_ERR
This bit indicates when the measured value of Y-axis becomes abnormal due to structural resonance in the sensor.
1: Measurement value is abnormal due to structural resonance
0: Measured value is within normal range

bit [5] Z_EXI_ERR
This bit indicates when the measured value of Z-axis becomes abnormal due to structural resonance in the sensor.
1: Measurement value is abnormal due to structural resonance
0: Measured value is within normal range

bit [4] XALARM_ERR
This bit indicates when the sensor value exceeds the value set in register: X_ALARM [0x47-0x46(W1)] in the X axis during measurement.
1: detection
0: no detection

bit [3] YALARM_ERR
This bit indicates when the sensor value exceeds the value set in register: Y_ALARM [0x49-0x48(W1)] in the Y axis during measurement.
1: detection
0: no detection

bit [2] ZALARM_ERR
This bit indicates when the sensor value exceeds the value set in register: Z_ALARM [0x4B-0x4A(W1)] in the Z axis

during measurement.
1: detection
0: no detection

bit [1] ALIASI_ERR(ALIASIng_ERRor)
This bit indicates the validation check of the combination setting of the output rate in register: SMPL_CTRL [0x04(W1)], bit [11:8] and filter cutoff frequency in register: FILTER_CTRL [0x06 (W1)], bit [3:0].
1: Abnormal Setting
0: Normal Setting

bit [0] EA (All Error) flag
When at least one failure is found in the diagnostic result (DIAG_STAT1 [0x04(W0)]), this bit is set to "1" (failure occurred). This bit is reset to "0" by reading the DIAG_STAT1 register.
1: Failure occurred
0: No Failure

6.5. COUNT Register (Window 0)

Internal Timer Measurement

Addr (Hex)	Bit15	…	Bit0	R/W
0x0A	SAMPLING_ COUNT			R

bit [15:0] SAMPLING_COUNT
This register returns the sampling count value of the internal Analog Front End.

Note) The time unit of the sampling counter value represents 250 µs/count.
Example: If the data output rate equals 1000Sps, the counter value sequence is 0, 4, 8, ... , 0xFFFC, 0, 4, ...

External Trigger Measurement

Addr (Hex)	Bit15	…	Bit0	R/W
0x0A	SAMPLING_ COUNT			R

bit [15:0] SAMPLING_COUNT
Reads the counter value for resampling triggered. Counts up by + 1 with each resampling.
Example: SAMPLING_COUNT = 0, 1, 2, … , 65535, 0, 1, …

1 PPS measurement

Addr (Hex)	Bit15	Bit14	…	Bit0	R/W
0x0A	1PPS_ COUNT	SAMPLING_ COUNT			R

bit [15] 1PPS_COUNT
Reads the 1-bit counter value of the 1 PPS signal.

bit [14:0] SAMPLING_COUNT
Reads the counter value for resampling triggered. Counts up by + 1 with each resampling.
Example: SAMPLING_COUNT = 0, 1, 2, … , 32767, 0, 1, …

6.6. DIAG_STAT2 Register (Window 0)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x0D	-	-	-	-	-	-	-	-	-

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x0C	-	-	Z_SENS _ERR		Y_ SENS _ERR		X_ SENS _ERR		R

Note) When the host reads the diagnosis result, all the results will be cleared to 0.

bit [5:4] Z_SENS_ERR (SENSitivity ERRor)

Shows the Z-axis execution result of **SENS_TEST** (Sensitivity Test) of MSC_CTRL [0x02 (W1)], bit [12].
11 : Unable to be determined (Excessive vibration level)
10 : Unable to be determined (Insufficient vibration level)
01 : Error occurred
00 : No error
If this error occurs, acceleration sensor is faulty.

bit [3:2] Y_SENS_ERR (SENSitivity ERRor)
Shows the Y-axis execution result of **SENS_TEST** (Sensitivity Test) of MSC_CTRL [0x02 (W1)], bit [12].
The execution result is the same as **Z_SENS_ERR**.

bit [1:0] X_SENS_ERR (SENSitivity ERRor)
Shows the X-axis execution result of **SENS_TEST** (Sensitivity Test) of MSC_CTRL [0x02 (W1)], bit [12].
The execution result is the same as **Z_SENS_ERR**.

6.7. TEMP Register (Window 0)

Addr (Hex)	Bit15	...	Bit0	R/W
0x0E	TEMP_HIGH			R
0x10	TEMP_LOW			R

bit [15:0] Temperature sensor output data
The internal temperature sensor value can be read from this register.
The output data format is 32-bit two's complement format.

Please refer to the below formula for conversion to temperature in centigrade. Please refer to Table 1.3 Sensor Specification for the scale factor value.There is no guarantee that the value provides the absolute value of the internal temperature.

$$T\ (°C) = SF \times a + 34.987$$

SF: Scale Factor
a: Temperature sensor output data (decimal)

6.8. ACCL Register (Window 0)

Addr (Hex)	Bit15	…	Bit0	R/W
0x30	XACCL_HIGH			R
0x32	XACCL_LOW			R
0x34	YACCL_HIGH			R
0x36	YACCL_LOW			R
0x38	ZACCL_HIGH			R
0x3A	ZACCL_LOW			R

bit [15:0] Acceleration sensor output data
These registers contain the 3-axis acceleration data for X, Y, and Z.
Register: SIG_CTRL [0x00 (W1)] provides the output mode selection **OUTPUT_SEL** of bit [7:5] to specify the acceleration data as either "acceleration" or "Tilt angle".

The output data format
Unit [G]
32-bit two's complement format
bit31 : sign
bit30~24 : integer
bit23~0 : decimal

Note) When the combination of output rate and filter cutoff frequency is "abnormal setting", reading acceleration sensor value responds with error code "0x64000000"
Note) When the acceleration value exceeds the preset threshold value, reading acceleration value responds with the threshold value. If the preset threshold values are set to + 10 G and - 10 G, the corresponding response is “0x0A000000” for + 10 G or more, and “0xF6000000” for - 10 G or less.

6.9. TILT Register (Window 0)

Addr (Hex)	Bit15	…	Bit0	R/W
0x3C	XTILT_HIGH			R
0x3E	XTILT_LOW			R
0x40	YTILT_HIGH			R
0x42	YTILT_LOW			R
0x44	ZTILT_HIGH			R
0x46	ZTILT_LOW			R

bit [15:0] Tilt sensor output data

These registers contain the 3-axis Tilt angle data for X, Y, and Z.
Register: SIG_CTRL [0x00 (W1)] The tilt angle is output only when the output mode selection **OUTPUT_SEL** of bit [7: 5] is set to "tilt angle".

The output data format
Unit (radian)
32-bit two's complement format
bit 31 : sign
bit 30 ~ 29 : integer
bit 28 ~ 0 : decimal

Note) When the combination of output rate and filter cutoff frequency is "abnormal setting", reading tilt angle sensor value responds with error code "0x64000000"
Note) When the tilt angle value exceeds the dynamic range (± 60 °), reading tilt angle value responds with the value of + 60 ° or - 60 °. The corresponding response is “0x2182A470” for + 60 ° or more, and “0xDE7D5B90” for - 60 ° or less.

6.10. SENTST_PW Register (Window 0)

Addr (Hex)	Bit15	…	Bit0	R/W
0x50	SENTST_PW_X_HIGH			R
0x52	SENTST_PW_X_LOW			R
0x54	SENTST_PW_Y_HIGH			R
0x56	SENTST_PW_Y_LOW			R
0x58	SENTST_PW_Z_HIGH			R
0x5A	SENTST_PW_Z_LOW			R

bit [15:0] Sensitivity test vibration level

The environmental vibration level during the sensitivity test for X, Y, and Z axes (unsigned 32-bit integer) can be read. If the environmental vibration level is outside the specified range, the diagnostic result in the DIAG_STAT2 register will indicate indeterminable status.

Out-of-Range Environmental Vibration Levels

Insufficient Vibration Level : Below 25,000
Excessive Vibration Level : Above typ. 500,000,000 *1

*1) The threshold for excessive vibration level varies depending on the sensitivity of each sensor. When exceeded, the response will be 0xFFFFFFFF.

6.11. SIG_CTRL Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x01	ND_EN (Temp)	-	-	-	ND_EN (XACCL) (XTILT)	ND_EN (YACCL) (YTILT)	ND_EN (ZACCL) (ZTILT)	-	R/W

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x00	OUTPUT_ SEL_X	OUTPUT_ SEL_Y	OUTPUT_ SEL_Z	-	-	-	-	-	R/W

bit [15] ND_EN (Temp)
Enables or disables the temperature sensor ND flags in FLAG [0x06(W0)], bit [15].
1: Enable
0: Disable

bit [11] ND_EN (X-axis sensor)
Enables or disables the X-axis sensor ND flags in FLAG [0x06(W0)], bit [11].
1: Enable
0: Disable

bit [10] ND_EN (Y-axis sensor)
Enables or disables the Y-axis sensor ND flags in FLAG [0x06(W0)], bit [10].
1: Enable
0: Disable

bit [9] ND_EN (Z-axis sensor)
Enables or disables the Z-axis sensor ND flags in FLAG [0x06(W0)], bit [9].
1: Enable
0: Disable

bit [7] OUTPUT_SEL_X
Sets the output mode on the X axis.
1: Tilt angle
0: Acceleration

bit [6] OUTPUT_SEL_Y
Sets the output mode on the Y axis.
1: Tilt angle
0: Acceleration

bit [5] OUTPUT_SEL_Z
Sets the output mode on the Z axis.
1: Tilt angle
0: Acceleration

6.12. MSC_CTRL Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x03	-	-	-	SENS _TEST	FLASH _TEST	ACC _TEST	TEMP _TEST	VDD _TEST	R/W

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x02	EXT _SEL		EXT _POL	-	-	DRDY _ON	DRDY _POL	-	R/W

Note) Although **ACC_TEST**, **TEMP_TEST**, and **VDD_TEST** can be executed at the same time, other tests cannot be executed at the same time. When executing them in succession, confirm the execution of the previous command is finished by waiting until the bit changes from “1” to “0” and then execute the next command.

bit [12] SENS_TEST
Write “1” to execute the self test to check if the X, Y, Z axis accelerometer sensitivity is working properly. The read value of the bit is “1” during the test and “0” after the test is completed. After writing “1” to this bit, wait until this bit goes back to “0” and then read the **X_SENS_ERR**, **Y_SENS_ERR**, **Z_SENS_ERR** of DIAG_STAT2 [0x0C(W0)], bit [5:0] to check the result.

bit [11] FLASH_TEST

Write “1” to execute the data consistency test for the non-volatile memory. The read value of the bit is “1” during the test and “0” after the test is completed. After writing “1” to this bit, wait until this bit goes back to “0” and then read the **FLASH_ERR** of DIAG_STAT1 [0x04(W0)], bit [2] to check the result.

Note) This flash memory test cannot be run with other tests at the same time.

bit [10] ACC_TEST
Write “1” to execute the self test to check if the X, Y, and Z axis sensor is working properly. The read value of the bit is “1” during the test and “0” after the test is completed. After writing “1” to this bit, wait until this bit goes back to “0” and then read the **ACC_ERR_ALL** of DIAG_STAT1 [0x04(W0)], bit [1] to check the results.

bit [9] TEMP_TEST
Write “1” to execute the self test to check if temperature sensor is working properly. The read value of the bit is “1” during the test and “0” after the test is completed. After writing “1” to this bit, wait until this bit goes back to “0” and then read the **TEMP_ERR** of DIAG_STAT1 [0x04(W0)], bit [9] to check the results.

bit [8] VDD_TEST
Write “1” to execute the self test to check if power supply voltage level is working properly. The read value of the bit is “1” during the test and “0” after the test is completed. After writing “1” to this bit, wait until this bit goes back to “0” and then read the **VDD_ERR** of DIAG_STAT1 [0x04(W0)], bit [8] to check the results.

bit [7:6] EXT_SEL
Select the function of the EXT terminal.
3: Reserved
2: 1 PPS singal input is enabled
1: External trigger input is enabled
0: Internal timer trigger is enabled

bit [5] EXT_POL
Selects the polarity of the EXT terminal (Recovery from Sleep Mode).
1: Negative logic (falling edge)
0: Positive logic (rising edge)

bit [2] DRDY_ON
Selects the function of the DRDY terminal, when set to “1”, Data Ready signal is output.
1: Data Ready Signal is enabled
0: Data Ready Signal is disabled

bit [1] DRDY_POL
Selects the polarity of the Data Ready signal when selected in **DRDY_ON** above.
1: Active High
0: Active Low

6.13. SMPL_CTRL Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x05	-	-	-	-	DOUT_RATE				R/W

Addr (Hex)	Bit7	…	Bit0	R/W
0x04	-			-

bit [11:8] DOUT_RATE
Specifies the data output rate. To avoid aliasing, refer to Table 4.4 Measurable output rate and cutoff frequency combination for output rate setting.
0000: Reserved
0001: Reserved
0010: 1,000Sps
0011: 500Sps
0100: 200Sps
0101: 100Sps
0110: 50Sps
0111-1111: not used

Note) The factory setting is ODR: 200 Hz

Note) The maximum output rate is limited to 500 Sps when long-term filter is used.

6.14. FILTER_CTRL Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x07	-	-	-	-	-	-	-	-	-

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x06	-	-	FILTER_ STAT	-	FILTER_SEL				R/W *1

*1) Only FILTER_STAT is read-only.

bit [5] FILTER_STAT

This read-only status bit shows the status of the filter setting
1: Filter setting is busy
0: Filter setting is completed

bit [3:0] FILTER_SEL

Specifies the type of filter,TAP setting and cutoff frequency.
For the FIR Kaiser filter, these bits also select the cutoff frequency. When using user defined FIR filter, please program the filter coefficient data

0000: Reserved
0001: FIR Kaiser Filter TAP = 64、fc = 83 Hz
0010: Reserved
0011: FIR Kaiser Filter TAP = 128、fc=36 Hz
0100: FIR Kaiser Filter TAP = 128、fc=110 Hz
0101: Reserved
0110: FIR Kaiser Filter TAP = 512、fc=9 Hz
0111: FIR Kaiser Filter TAP = 512、fc=16 Hz
1000: FIR Kaiser Filter TAP = 512、fc=60 Hz
1001: FIR Kaiser Filter TAP = 512、fc=210 Hz
1010: Reserved
1011: User Defined FIR Filter TAP = 4 Hz
1100: User Defined FIR Filter TAP = 64 Hz
1101: User Defined FIR Filter TAP = 128 Hz
1110: User Defined FIR Filter TAP = 512 Hz
1111: not used

After writing to this bit, FILTER_STAT changes to 1 (during execution).
Confirm the completion of the filter setting process by confirming that the FILTER_STAT bit returns to "0".

Note) For the combination of output rate and cutoff frequency considering avoidance of aliasing and transient response at sampling start, refer to 4.17.3 Notes on FIR filter.

Note) The factory settings are Tap: 512, Fc: 60 Hz

6.15. UART_CTRL Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x09	-						BAUD_RATE		R/W

Addr (Hex)	Bit7	…	Bit2	Bit1	Bit0	R/W
0x08	-			AUTO _START	UART _AUTO	R/W

bit [9:8] BAUD_RATE

These bits specifies the Baud Rate of UART interface.
00: Reserved

01: 460.8 kbps
10: 230.4 kbps
11: 115.2 kbps

Note) The baud rate change using these **BAUD_RATE** bits become effective immediately after write access completes.

bit [1] AUTO_START (Only valid for UART Auto sampling)
Enables or disables the Auto Start function.
1: Automatic Start is enabled
0: Automatic Start is disabled
When Auto Start is enabled, the device enters sampling mode and sends sampling data automatically after completing internal initialization after powered on.
Write a "1" to this **AUTO_START** bit and **UART_AUTO** bit of this register to enable this function. Then execute **FLASH_BACKUP** of GLOB_CMD [0x0A(W1)], bit [3] to preserve the current register settings.

bit [0] UART_AUTO
Enables or disables the UART Auto sampling function.
1: UART Auto sampling is selected
0: UART Manual sampling is selected
If UART Auto sampling is active, register values such as flag, temperature, and acceleration are continuously transmitted automatically according to the data output rate set by SMPL_CTRL [0x04(W1)] register. In UART Manual sampling, register data is transmitted as a response to a register read command.

Note) This register bit must be set to 0 when using the SPI interface.
Note) For more info on UART Auto sampling refer to 5.2.4 UART Auto Sampling Operation and 5.3 Data Packet Format. The burst output data is configured by register setting in BURST_CTRL [0x0C(W1)].

6.16. GLOB_CMD Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x0B	-	-	-	-	-	NOT _READY	-	-	R

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x0A	SOFT _RST	-	-	-	FLASH_ BACKUP	FLASH _RST	-	-	R/W

bit [10] NOT_READY
Indicates whether this product currently ready. Immediately after power on, this bit is “1” and becomes “0” when the product is ready. After the power on, wait until the Power-On Start-Up Time has elapsed and then wait until this bit becomes “0” before starting sensor measurement. This bit is read-only.
1: Not ready
0: Ready

bit [7] SOFT_RST
Write “1” to execute software reset, and wait until the Reset Recovery Time has elapsed. After the software reset is completed, the bit automatically goes back to “0”.

bit [3] FLASH_BACKUP
Write “1” to save the current values of the control registers with the ○ mark in the “Flash Backup” column of Table 6.1 to the non-volatile memory. After the execution is completed, the bit automatically goes back to “0”. After confirming this bit goes back to “0” and then check the result in **FLASH_BU_ERR** of DIAG_STAT1 [0x04(W0)], bit [0].

bit [2] FLASH_RST
Write “1” to resets the setting value saved in the nonvolatile memory to the factory default state. After completion of execution, it will automatically return to “0”. After confirming this bit goes back to “0” and then check the result in **FLASH_BU_ERR** of DIAG_STAT1 [0x04(W0)], bit [0]. The factory default state will be reflected to the registers after completing internal initialization after powered on or a reset.

6.17. BURST_CTRL Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x0D	FLAG _OUT	TEMP _OUT	-	-	-	ACCX _OUT	ACCY _OUT	ACCZ _OUT	R/W

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x0C	-	-	-	-	-	-	COUNT _OUT	CHKSM _OUT	R/W

These bits enable/disable the content in the output data for burst mode and UART Auto sampling.

bit [15] FLAG_OUT
Controls the output of FLAG status.
1: Enables output.
0: Disables output.

bit [14] TEMP_OUT
Controls the output of temperature.
1: Enables output.
0: Disables output.

bit [10] ACCX_OUT
Controls the output of X axis acceleration / tilt angle. The output mode is selected by **OUTPUT_SEL_X** of register: SIG_CTRL [0x00 (W1)], bit [7].
1: Enables output.
0: Disables output.

bit [9] ACCY_OUT
Controls the output of Y axis acceleration / tilt angle. The output mode is selected by **OUTPUT_SEL_Y** of register: SIG_CTRL [0x00 (W1)], bit [6].
1: Enables output.
0: Disables output.

bit [8] ACCZ_OUT
Controls the output of Z axis acceleration / tilt angle. The output mode is selected by **OUTPUT_SEL_Z** of register: SIG_CTRL [0x00 (W1)], bit [5].
1: Enables output.
0: Disables output.

bit [1] COUNT_OUT
Controls the output of counter value.
1: Enables output.
0: Disables output.

bit [0] CHKSM_OUT
Controls the output of checksum.
1: Enables output.
0: Disables output.

Note) Please set "1: Enables output" to at least one bit of bit [8:10]. All outputs of acceleration / tilt angle values cannot be desabled at the same time.

6.18. FIR_UCMD Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x17	-	-	-	-	-	-	-	-	-

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x16	-	-	-	-	-	-	FIR_UCMD		R/W

bit [1:0] FIR_UCMD (FIR Filter User CoMmanD)
These bits set the control command for setting the coefficient data of the user defined FIR filter.
READ WRITE

00: execution complete	do not execute
01: reading in progress	read
10: writing in progress	write
11: not used	not used

6.19. FIR_UDATA Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x19	DATA _ERR	-	-	-	-	-	-	-	R

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x18	FIR_UDATA								R/W

bit [15] DATA_ERR

This bit shows the state of the read error on the coefficient data of the user defined FIR filter.

1: Read error

0: Normal operation

bit [7:0] FIR_UDATA(FIR Filter User DATA)

Set the coefficient data (binary) of the user defined FIR filter.

6.20. FIR_UADDR Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x1B	FIR_UADDR _HIGH								R/W

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x1A	FIR_UADDR _LOW								R/W

bit [15:8] FIR_UADDR_HIGH

Upper address of the coefficient data of the user FIR filter.

bit [7:0] FIR_UADDR_LOW

Lower address of the coefficient data of the user FIR filter.

Note) This address is automatically incremented after the read / write command is executed.

Note) The setting range is from 0x0800 to 0x0FFF. It cannot be set outside the range.

6.21. LONGFILT_CTRL Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x1D	-	-	-	-	-	-	-	-	-

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x1C	-	-	-	-	-	-	0	FILT_EN	R/W[*1]

bit [0] FILT_EN

This bit enable / disable long-period filter.

1: Enable
0: Disable

6.22. LONGFILT_TAP Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x1F	-	-	-	-	-	-	-	-	-

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x1E	-	-	-	-	TAP_SIZE				R/W

bit [3:0] TAP_SIZE
These bits set the tap size of the long period filter.
Number of taps = 2^{TAP_SIZE}

Note) The setting range of TAP_SIZE is from 2 to 12.

6.23. XA_OFFSET Register (Window 1)

Addr (Hex)	Bit15	…	Bit0	R/W
0x2C	XOFFSET_HIGH			R/W

bit [15:0] XOFFSET_HIGH
Sets the X-axis acceleration offset value upper word.

Addr (Hex)	Bit15	…	Bit0	R/W
0x2E	XOFFSET_LOW			R/W

bit [15:0] XOFFSET_LOW
Sets the X-axis acceleration offset value lower word.

6.24. YA_OFFSET Register (Window 1)

Addr (Hex)	Bit15	…	Bit0	R/W
0x30	YOFFSET_HIGH			R/W

bit [15:0] YOFFSET_HIGH
Sets the Y-axis acceleration offset value upper word.

Addr (Hex)	Bit15	…	Bit0	R/W
0x32	YOFFSET_LOW			R/W

bit [15:0] YOFFSET_LOW
Sets the Y-axis acceleration offset value lower word.

6.25. ZA_OFFSET Register (Window 1)

Addr (Hex)	Bit15	…	Bit0	R/W
0x34	ZOFFSET_HIGH			R/W

bit [15:0] ZOFFSET_HIGH
Sets the Z-axis acceleration offset value upper word.

Addr (Hex)	Bit15	…	Bit0	R/W
0x36	ZOFFSET_LOW			R/W

bit [15:0] ZOFFSET_LOW
Sets the Z-axis acceleration offset value lower word.

6.26. X_ALARM Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x47	XALARM _UP								R/W

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x46	XALARM _LO								R/W

bit [15:8] XALARM_UP
Sets the acceleration upper limit value to be determined by **XALARM_ERR** of register: FLAG [0x06 (W0)], bit [4].
Data format : 8-bit, two's complement format
Setting Unit : G
Setting range : - 10 to + 10 (can not be set to a value outside the range)

bit [7:0] XALARM_LO
Sets the acceleration lower limit value to be determined by **XALARM_ERR** of register: FLAG [0x06 (W0)], bit [4].
The data format and setting range are the same as those of **XALARM_UP**.

6.27. Y_ALARM Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x49	YALARM _UP								R/W

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x48	YALARM _LO								R/W

bit [15:8] YALARM_UP
Sets the acceleration upper limit value to be determined by **YALARM_ERR** of register: FLAG [0x06 (W0)], bit [3].
The data format and setting range are the same as those of **XALARM_UP**.

bit [7:0] YALARM_LO
Sets the acceleration lower limit value to be determined by **YALARM_ERR** of register:FLAG [0x06 (W0)], bit [3].
The data format and setting range are the same as those of **XALARM_UP**.

6.28. Z_ALARM Register (Window 1)

Addr (Hex)	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	R/W
0x4B	ZALARM _UP								R/W

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W
0x4A	ZALARM _LO								R/W

bit [15:8] ZALARM_UP
Sets the acceleration upper limit value to be determined by **ZALARM_ERR** of register: FLAG [0x06 (W0)], bit [2].
The data format and setting range are the same as those of **XALARM_UP**.

bit [7:0] ZALARM_LO
Sets the acceleration lower limit value to be determined by **ZALARM_ERR** of register: FLAG [0x06 (W0)], bit [2].
The data format and setting range are the same as those of **XALARM_UP**.

6.29. PROD_ID Register (Window 1)

Addr (Hex)	Bit15	…	Bit0	R/W
0x6A	PROD_ID1			R
0x6C	PROD_ID2			R
0x6E	PROD_ID3			R
0x70	PROD_ID4			R

bit [15:0] Product ID
These registers return the product model number represented in ASCII code.

Product ID return value is A370AD10
PROD_ID1: 0x3341
PROD_ID2: 0x3037
PROD_ID3: 0x4441
PROD_ID4: 0x3031

6.30. VERSION Register (Window 1)

Addr (Hex)	Bit15	…	Bit0	R/W
0x72	VERSION			R

bit [15:0] Version
This register returns the Firmware Version.

6.31. SERIAL_NUM Register (Window 1)

Addr (Hex)	Bit15	…	Bit0	R/W
0x74	SERIAL_NUM1			R
0x76	SERIAL_NUM2			R
0x78	SERIAL_NUM3			R
0x7A	SERIAL_NUM4			R

bit [15:0] Serial Number
These registers return the serial number represented in ASCII code.

For example, if the Serial Number is 01234567 then the return value is:
SERIAL_NUM1: 0x3130
SERIAL_NUM2: 0x3332
SERIAL_NUM3: 0x3534
SERIAL_NUM4: 0x3736

6.32. WIN_CTRL Register (Window 0,1)

Addr (Hex)	Bit15	…	Bit8	R/W
0x7F	-			-

Addr (Hex)	Bit7	…	Bit0	R/W
0x7E	WINDOW_ID			R/W

bit [7:0] WINDOW_ID

Selects the desired register window by writing the window number to this register.
0x00: Window 0
0x01: Window 1
0x02 ~ 0xFF: Unused

7. Sample Program Sequence

The following describes the recommended procedures for operating this device.

7.1. UART Sample Programs

7.1.1. Power-On Sequence (UART)

(a) Power on.
(b) Wait for the time specified by "Power-On Start-Up Time".
(c) Check **NOT_READY** in register: GLOB_CMD [0x0A(W1)], bit [10].
Tx = {0xFE, 0x01, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 1 */
Tx = {0x0A, 0x00, 0x0d}. /* Read out GLOB_CMD */
Rx = {0x0A, MSByte, LSByte, 0x0d}. /* Retrieve the response value */
// if **NOT_READY** is 0, initialization is complete; if 1, initialization is in progress.
(d) Check **HARD_ERR** in register: DIAG_STAT1 [0x04(W0)], bit [7:5].
Tx = {0xFE,0x00,0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 0 */
Tx = {0x04,0x00,0x0d}. /* Read out DIAG_STAT1 */
Rx = {0x04,MSByte,LSByte,0x0d}. /* Retrieve the response value */
// If **HARD_ERR** is 000, the hardware check completes successfully; if not, an error occurred.

7.1.2. Register Read and Write (UART)

Register Read Example

(a) Read 16-bit data from the register (Address = 0x02 / Window = 0).
Tx = {0xFE, 0x00, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW**_ID = 0 */
Tx = {0x02, 0x00, 0x0d}. /* Read out MODE_CTRL */
Rx = {0x02, 0x04, 0x00, 0x0d}. /* Retrieve the response value */
// The 2nd byte of Rx data “0x04” indicates a configuration mode.
// The 3rd byte of Rx data “0x00” indicates Reserved.
// Read data is by 16 bits with MSB first format.

Register Write Example

(a) Write 8-bit data to the register (Address = 0x03 / Window = 0).
Tx = {0xFE, 0x00, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 0 */
Tx = {0x83, 0x01, 0x0d}. /* Write to MODE_CTRL (H) to go to Sampling mode */
// No corresponding response for data writing.
// Write data is by 8 bits

7.1.3. Sampling (UART)

Auto sampling (example)

(a) Configure the sampling parameters (the following is an example of setting the factory defaults).
Tx = {0xFE, 0x01, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 1 */
Tx = {0x80, 0x00, 0x0d}. /* Write to SIG_CTRL (L) to set output physical quantity = Acceleration */
Tx = {0x85, 0x04, 0x0d}. /* Write to SMPL_CTRL (H) to set data output rate = 200Sps */
Tx = {0x86, 0x08, 0x0d}. /* Write to FILTER_CTRL (L) to set FIR filter = 512 tap, 60 Hz */
Tx = {0x88, 0x01, 0x0d}. /* Write to UART_CTRL (L) to set UART Mode = Auto sampling*/
Tx = {0x8C, 0x02, 0x0d}. /* Write to BURST_CTRL (L) to set Burst counter = on、checksum = off */
Tx = {0x8D, 0x47, 0x0d}. /* Write to BURST_CTRL (H) to set Burst flag = off、temp = on、sensor = on */
Tx = {0xFE, 0x00, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 0 */
(b) Start sampling.
Tx = {0x83, 0x01, 0x0d}. /* Write to MODE_CTRL (H) to go to Sampling mode */
// Note) The transition duration from Configuration mode to Sampling mode, refer to “Sampling Start Time” in Table 1.4 Interface Specifications.
// Note) The transient response time (output hold time) of FIR filters, refer to Table 4.3.
(c) Receive sampling data.
Rx = {0x80,
TEMP_HIGH_H, TEMP_HIGH_L, TEMP_LOW_H, TEMP_LOW_L,
XACCL_HIGH_H, XACCL_HIGH_L, XACCL_LOW_H, XACCL_LOW_L,
YACCL_HIGH_H, YACCL_HIGH_L, YACCL_LOW_H, YACCL_LOW_L,
ZACCL_HIGH_H, ZACCL_HIGH_L, ZACCL_LOW_H, ZACCL_LOW_L,
COUNT_H, COUNT_L,
0x0d}

```
  // Repeat (c).
  // “XACCL_HIGH_H” refers to the MSB byte of XACCL_HIGH data
  // “XACCL_HIGH_L” refers to the LSB byte of XACCL_HIGH data
  // “XACCL_LOW_H” refers to the MSB byte of XACCL_LOW data
  // “XACCL_LOW_L” refers to the LSB byte of XACCL_LOW data
(d) Stop sampling.
  Tx = {0x83, 0x02, 0x0d}.          /* Write to MODE_CTRL (H) to go to Configuration mode */
  // Note) For the transition duration from Sampling mode to Configuration mode, refer to “Sampling Stop Time” in Table 1.4
          Interface Specifications.
```

Burst mode sampling (example)

```
(a) Configure the sampling parameters.
  // Tilt angle, temperature, flag, sampling counter value, checksum (output of all available data)
  Tx = {0xFE, 0x01, 0x0d}.          /* Write to WIN_CTRL (L) to set WINDOW_ID = 1 */
  Tx = {0x80, 0xE0, 0x0d}.          /* Write to SIG_CTRL (L) to set output physical quantity = Tilt angle */
  Tx = {0x85, 0x04, 0x0d}.          /* Write to SMPL_CTRL (H) to set data output rate = 200Sps */
  Tx = {0x86, 0x08, 0x0d}.          /* Write to FILTER_CTRL (L) to set FIR filter = 512 tap, 60 Hz */
  Tx = {0x88, 0x00, 0x0d}.          /* Write to UART_CTRL (L) to set UART Mode = manual sampling*/
  Tx = {0x8C, 0x03, 0x0d}.          /* Write to BURST_CTRL (L) to set Burst counter = on, checksum = on */
  Tx = {0x8D, 0xC7, 0x0d}.          /* Write to BURST_CTRL (H) to set Burst flag = on, temp = on, sensor = on */
  Tx = {0xFE, 0x00, 0x0d}.          /* Write to WIN_CTRL (L) to set WINDOW_ID = 0 */
(b) Start sampling.
  Tx = {0x83, 0x01, 0x0d}.          /* Write to MODE_CTRL (H) to go to Sampling mode */
  // Note) For the transition duration from Configuration mode to Sampling mode, refer to “Sampling Start Time” in Table 1.4
          Interface Specifications.
  // Note) The transient response time (output hold time) of FIR filters, refer to Table 4.3.
(c) A burst command is sent when Data Ready signal is asserted.
  Tx = {0x80, 0x00, 0x0d}.          /* Write to BURST (L) */
(d) Retrieve sampling data.
  Rx = {0x80,
        FLAG_H, FLGA_L,
        TEMP_HIGH_H, TEMP_HIGH_L, TEMP_LOW_H, TEMP_LOW_L,
        XTILT_HIGH_H, XTILT_HIGH_L, XTILT_LOW_H, XTILT_LOW_L,
        YTILT_HIGH_H, YTILT_HIGH_L, YTILT_LOW_H, YTILT_LOW_L,
        ZTILT_HIGH_H, ZTILT_HIGH_L, ZTILT_LOW_H, ZTILT_LOW_L,
        COUNT_H, COUNT_L,
        CHECKSUM_H, CHECKSUM_L,
        0x0d}
  // Repeat (c) and (d).
(e) Stop sampling.
  Tx = {0x83, 0x02, 0x0d}.          /* Write to MODE_CTRL (H) to go to Configuration mode */
  // Note) For the transition duration from Sampling mode to Configuration mode, refer to “Sampling Stop Time” in Table 1.4
          Interface Specifications.
```

7.1.4. Self Test (UART)

Data Consistency Test in Nonvolatile Memory (Flash Test)

```
(a) Perform a Flash test.
  Tx = {0xFE, 0x01, 0x0d}.          /* Write to WIN_CTRL (L) to set WINDOW_ID = 1 */
  Tx = {0x83, 0x08, 0x0d}.          /* Write to MSC_CTRL (H) to set FLASH_TEST = 1 */
(b) Wait until the test is completed.
  // Wait for the time specified in “Self Test Time (Flash Test)”.
  // Or verify FLASH_TEST of register: MSC_CTRL [0x02(W1)], bit [11] returns to 0 as shown below.
  Tx = {0x02, 0x00, 0x0d}.          /* Read out MSC_CTRL */
  Rx = {0x02, MSByte, LSByte, 0x0d}.  /* Retrieve the response value */
  // if FLASH_TEST is 0, the test is complete; if 1, repeat (b) since the tests in progress.
(c) Confirm the test results
  // Check FLASH_ERR in register: DIAG_STAT1 [0x04(W0)], bit [2]
  Tx = {0xFE, 0x00, 0x0d}.          /* Write to WIN_CTRL (L) to set WINDOW_ID = 0 */
  Tx = {0x04, 0x00, 0x0d}.          /* Read out DIAG_STAT1 */
  Rx = {0x04, MSByte, LSByte, 0x0d}.  /* Retrieve the response value */
  // if FLASH_ERR is 0, the diagnosis result is OK; if 1, the diagnosis result is NG.
  // Note) This Flash test cannot be run with other tests at the same time.
```

Acceleration value test, Temperature value test, Power supply voltage level test

(a) Acceleration value test, Temperature value test, Power supply voltage level test are performed simultaneously.

Tx = {0xFE, 0x01, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 1 */
Tx = {0x83, 0x07, 0x0d}. /* Write to MSC_CTRL (H) to set **ACC_TEST/TEMP_TEST/VDD_TEST** = 1 */
(b) Wait until the tests are completed.
// Wait for the time specified in “Self Test Time (ACC Test , TEMP Test , VDD Test)”.
// Or verify **ACC_TEST/TEMP_TEST/VDD_TEST** of regster: MSC_CTRL [0x02(W1)], bit [10:8] return to 0 as shown below.
Tx = {0x02, 0x00, 0x0d}. /* Read out MSC_CTRL */
Rx = {0x02, MSByte, LSByte, 0x0d}. /* Retrieve the response value */
// if any of **ACC_TEST/TEMP_TEST/VDD_TEST** is 0, the tests are complete; if any of them is 1, repeat (b) since the corresponding test is in progress.
(c) Confirm the test results
// Check **TEMP_ERR/VDD_ERR/ACC_ERR_ALL** in register: DIAG_STAT1 [0x04(W0)], bit [9,8,1].
Tx = {0xFE, 0x00, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 0 */
Tx = {0x04, 0x00, 0x0d}. /* Read out DIAG_STAT1 */
Rx = {0x04, MSByte, LSByte, 0x0d}. /* Retrieve the response value */
// if any of **TEMP_ERR/VDD_ERR/ACC_ERR_ALL** is 0, the diagnosis results are OK; if any of them is 1, the diagnosis result for the corresponding test is NG.

Sensitivity test

(a) Perform the sensitivity test.
Tx = {0xFE, 0x01, 0x0d}. /* Write to WIN_CTRL (L), **WINDOW_ID** = 1 */
Tx = {0x83, 0x10, 0x0d}. /* Write to MSC_CTRL (H), **SENS_TEST** = 1 */
(b) Wait until the test is completed.
// Wait for the time specified in “Self Test Time (Sensitivity Test)”.
// Or verify that **SENS_TEST** of MSC_CTRL [0x02(W1)], bit [15] returns to 0 as shown below.
Tx = {0x02, 0x00, 0x0d}. /* Read MSC_CTRL */
Rx = {0x02, MSByte, LSByte, 0x0d}. /* Retrieve the response value */
// If **SENS_TEST** is 0, the test is complete; if 1, repeat (b) as the test is still in progress.
(c) Confirm the test results.
// Check **X_SENS_ERR**, **Y_SENS_ERR**, **Z_SENS_ERR** values in DIAG_STAT2 [0x0C(W0)], bit [5-0].
Tx = {0xFE, 0x00, 0x0d}. /* Write to WIN_CTRL (L), **WINDOW_ID** = 0 */
Tx = {0x0C, 0x00, 0x0d}. /* Read DIAG_STAT2 */
Rx = {0x0C, MSByte, LSByte, 0x0d}. /* Retrieve the response value */
// If **X_SENS_ERR**, **Y_SENS_ERR**, **Z_SENS_ERR** are 00, the assessment is OK; if 01, the assessment is NG.
// Note) Sensitivity test cannot be run simultaneously with other tests.

7.1.5. Software Reset (UART)

(a) Execute a software reset.
Tx = {0xFE, 0x01, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 1 */
Tx = {0x8A, 0x80, 0x0d}. /* Write to GLOB_CMD (L) to set **SOFT_RST** = 1 */
(b) Wait until the software reset is finished.
// Wait for the time specified in “Reset Recovery Time”.

7.1.6. Non-Volatile Memory Backup (UART)

(a) Backup the current register setting values to non-volatile memory.
Tx = {0xFE, 0x01, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 1 */
Tx = {0x8A, 0x08, 0x0d}. /* Write to GLOB_CMD (L) to set **FLASH_BACKUP** = 1 */
(b) Wait until the backup is completed.
// Wait for the time specified in “Flash Backup Time”.
// Or verify **FLASH_BACKUP** of register: GLOB_CMD[0x0A(W1)], bit [3] returns to 0 as shown below.
Tx = {0x0A, 0x00, 0x0d}. /* Read out GLOB_CMD */
Rx = {0x0A, MSByte, LSByte, 0x0d}. /* Retrieve the response value */
// if **FLASH_BACKUP** is 0, the backup is complete; if 1, repeat (b) since the backup is in progress.
(c) Confirm the backup result.
// Check **FLASH_BU_ERR** in register: DIAG_STAT1 [0x04(W0)], bit [0].
Tx = {0xFE, 0x00, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 0 */
Tx = {0x04, 0x00, 0x0d}. /* Read out DIAG_STAT1 */
Rx = {0x04, MSByte, LSByte, 0x0d}. /* Retrieve the response value */
// if **FLASH_BU_ERR** is 0, the backup completes successfully; if 1, an error occurred.

7.1.7. Non-Volatile Memory Reset (UART)

(a) Restores the register setting values in non-volatile memory to the factory defaults.
Tx = {0xFE, 0x01, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 1 */
Tx = {0x8A, 0x04, 0x0d}. /* Write to GLOB_CMD (L) to set **FLASH_RST** = 1 */
(b) Wait until the memory reset is completed.

// Wait for the time specified in “Flash Reset Time”.
// Or verify **FLASH_RST** of register: GLOB_CMD [0x0A(W1)], bit [2] returns to 0 as shown below.
Tx = {0x0A, 0x00, 0x0d}. /* Read out GLOB_CMD */
Rx = {0x0A, MSByte, LSByte, 0x0d}. /* Retrieve the response value */
// if **FLASH_RST** is 0, the reset is complete; if 1, repeat (b) since the reset is in progress.
(c) Confirm the reset result.
// Check **FLASH_BU_ERR** in register: DIAG_STAT1 [0x04(W0)], bit [0].
Tx = {0xFE, 0x00, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 0 */
Tx = {0x04, 0x00, 0x0d}. /* Read out DIAG_STAT1 */
Rx = {0x04, MSByte, LSByte, 0x0d}. /* Retrieve the response value */
// if **FLASH_BU_ERR** is 0, the reset is finished successfully; if 1, an error occurred.
(d) Reboot or reset the device.

7.1.8. Sleep Sequence (UART)

(a) Go to sleep mode.
Tx = {0xFE, 0x00, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 0 */
Tx = {0x83, 0x03, 0x0d}. /* Write to MODE_CTRL (H) to go to sleep mode */
(b) Wake up from sleep mode by detecting an edge trigger on the EXT pin.
// Input an edge trigger on the EXT pin.
// Note) UART communication is not available in sleep mode.
(c) Wait until the transition to the configuration mode is complete.
// Wait for the time specified in “Sleep Wake-up Time”.

7.1.9. Auto Start (UART only)

(a) Enable an Auto start function.
Tx = {0xFE, 0x01, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 1 */
Tx = {0x88, 0x03, 0x0d}. /* Write to UART_CTRL (L) to satisfy **AUTO_START・UART_AUTO** = 1 */
(b) Execute a non-volatile memory backup, see Chapter 7.1.6.
(c) Reboot or reset the device.
(d) Wait for the time specified in “Power-On Start-Up Time / Reset Recovery Time”.
(e) Transmission of sampling data will start automatically.

7.1.10. UART Communication Baud Rate Setting (UART only)

(a) Change the UART communication baud rate from 460.8 kbps (factory default setting) to 230.4 kbps.
Tx = {0xFE, 0x01, 0x0d}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 1 */
Tx = {0x89, 0x02, 0x0d}. /* Write to UART_CTRL (H) to set **BAUD_RATE** = “10” */
// Note) The configured baud rate is effective immediately after writing.
(b) Change the communication baud rate of the host to 230.4 kbps, and restart UART communication.
(c) To keep the communication baud rate of the device after reboot, perform a non-volatile memory backup, see chapter 7.1.6.

7.2. SPI Sample Programs

To use SPI interface, disable a UART Auto mode. Other operating procedures are the same as those for UART. The basic operation examples are shown below.

7.2.1. Disable UART Auto Mode (SPI)

(a) Disable a UART Auto mode.
Tx = {0xFE01} / Rx = {0x----}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 1 */
Tx = {0x8800} / Rx = {0x----}. /* Write to UART_CTRL (L) to satisfy **AUTO_START・UART_AUTO** = 0 */
// -: don't care

7.2.2. Register Read and Write (SPI)

Register Read Example

(a) Read 16-bit data from the register (Address = 0x02 / Window = 0).
Tx = {0xFE00} / Rx = {0x----}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 0 */
Tx = {0x0200} / Rx = {0x----}. /* Read out MODE_CTRL */
Tx = {0x----} / Rx = {0x0400}. /* Retrieve the response value */
// -: don't care
// High byte of Rx data “0x04” indicates a configuration mode.
// Low byte of Rx data “0x00” indicates Reserved.

// Read data is by 16 bits with MSB first format.

Register Write Example

(a) Write 8-bit data to the register (Address=0x03 / Window =0).

Tx = {0xFE00} / Rx = {0x----}. /* Write to WIN_CTRL (L) to set **WINDOW_ID** = 0 */

Tx = {0x8301} / Rx = {0x----}. /* Write to MODE_CTRL (H) to go to sampling mode. */

// -: don't care

// No corresponding response for data writing.

// Write data is by 8 bits

8. Handling Notes

8.1. Prohibited Handling

- Do not use the product if it has been dropped or subjected to excessive impact from tools such as hammers or electric screwdrivers. This product contains a microfabricated quartz oscillator. Excessive mechanical shock may result in failure or significantly increase the risk of malfunction.
- Inserting or removing the product's header and socket while power is applied may cause permanent damage. Always perform insertion and removal operations with the power turned off.
- Inserting the product's header into the socket in the wrong orientation may cause permanent damage. Ensure correct alignment and orientation when connecting the header and socket.
- Do not turn off the power while the product is accessing its non-volatile memory. Doing so may result in malfunction.
- Applying overcurrent or electrostatic discharge (ESD) to the product may cause permanent damage. During assembly, ensure that all equipment, tools, and personnel are properly grounded and that no high-voltage leakage occurs.

8.2. Cautions

8.2.1. General

- Before using this product, always verify its performance under actual operating conditions in the intended application environment.
- Ensure that sufficient safety measures are implemented in the equipment incorporating this product.
- Do not modify or disassemble this product.
- This product is not intended for general consumer use. Please ensure appropriate and safe handling by the user.
- This product is not designed for use in equipment requiring extremely high reliability where failure may pose a threat to human life or property (e.g., aerospace equipment, submarine repeaters, nuclear control systems, life-support systems, medical devices, transportation control systems, etc.). Seiko Epson Corporation assumes no responsibility for any damages resulting from the use of this product in such applications.
- This product is not designed to be radiation-resistant.
- The absolute maximum ratings are the limits that must not be exceeded under any circumstances. Exceeding these ratings may result in irreversible damage to the product.
- Glossy marks may appear on the product casing due to adhesive materials used in the manufacturing process. These marks do not affect the product's functionality or quality.
- A parting line may appear on one side of the product casing as a result of the molding process. This is not a defect.

8.2.2. Handling Precautions

- When installing or removing this product, do not inadvertently turn the assembly screws. Performance and quality cannot be guaranteed for products whose assembly screws have been manipulated.
- When mounting this product to a case, equipment, or jig, ensure that no mechanical stress such as warping or twisting is applied. Secure the product with screws firmly enough to prevent damage to the mounting section, and apply anti-loosening measures as necessary.
- Ensure that no conductive materials such as metal fragments enter the product during installation. Intrusion of conductive materials may cause malfunction or damage.
- This product contains internal capacitors on the power line, which may cause inrush current at power-on. Depending on the system configuration, this may result in a significant voltage drop. Please evaluate thoroughly under actual operating conditions before use.
- During operation, excessive external noise may cause degradation in accuracy, malfunction, or damage. Implement appropriate noise suppression or isolation measures at the system level.
- The self-diagnostic test function in this sensor is designed to detect internal device faults. However, it cannot detect minor performance degradation due to long-term use or minor failures. If any abnormality in sensor performance is observed, discontinue use even if the self-diagnostic test passes.
- If a wireless device (transmitting antenna) is installed near this product, accuracy may degrade due to radio wave interference. Install the product away from such devices or apply shielding to block radio waves.
- Mechanical vibration, shock, continuous stress, or rapid temperature changes may cause cracks or disconnections at various joints.
- If environmental vibration is expected near the product's resonance frequency, evaluate thoroughly before use.
- In general, when a vibration sensor is mounted to a target machine, contact-induced resonance may occur. In particular, if the mounting is loose, such resonance can degrade measurement accuracy. To prevent this, it is recommended to secure the product firmly using screws.
- If water enters the product, it may cause malfunction or damage. If there is a risk of water exposure, ensure the system is waterproof. Operation is not guaranteed under conditions of condensation, dust, oil, corrosive gases (e.g., salt, acid, alkali),

or direct sunlight.

8.2.3. Storage and Transportation

- Avoid applying shock, vibration, or water exposure to the packaging box. Store and use the product in an environment that prevents condensation due to rapid temperature changes.
- To minimize characteristic changes during long-term storage, it is recommended to store the product under normal temperature and humidity conditions: + 5 °C to + 35 °C, 45 %RH to 85 %RH (JIS Z 8703).
- Avoid storage in environments with high temperature, high humidity, direct sunlight, corrosive gases, or excessive dust.
- Do not apply mechanical load to the product during storage.
- Ensure that the final packaging and transportation containers for the finished product are designed to prevent excessive vibration or shock.

8.3. Product Warranty

- The warranty period for this product is 12 months from the date of shipment.
- During the warranty period, if any defect attributable to our company is found, we will replace the product free of charge.

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